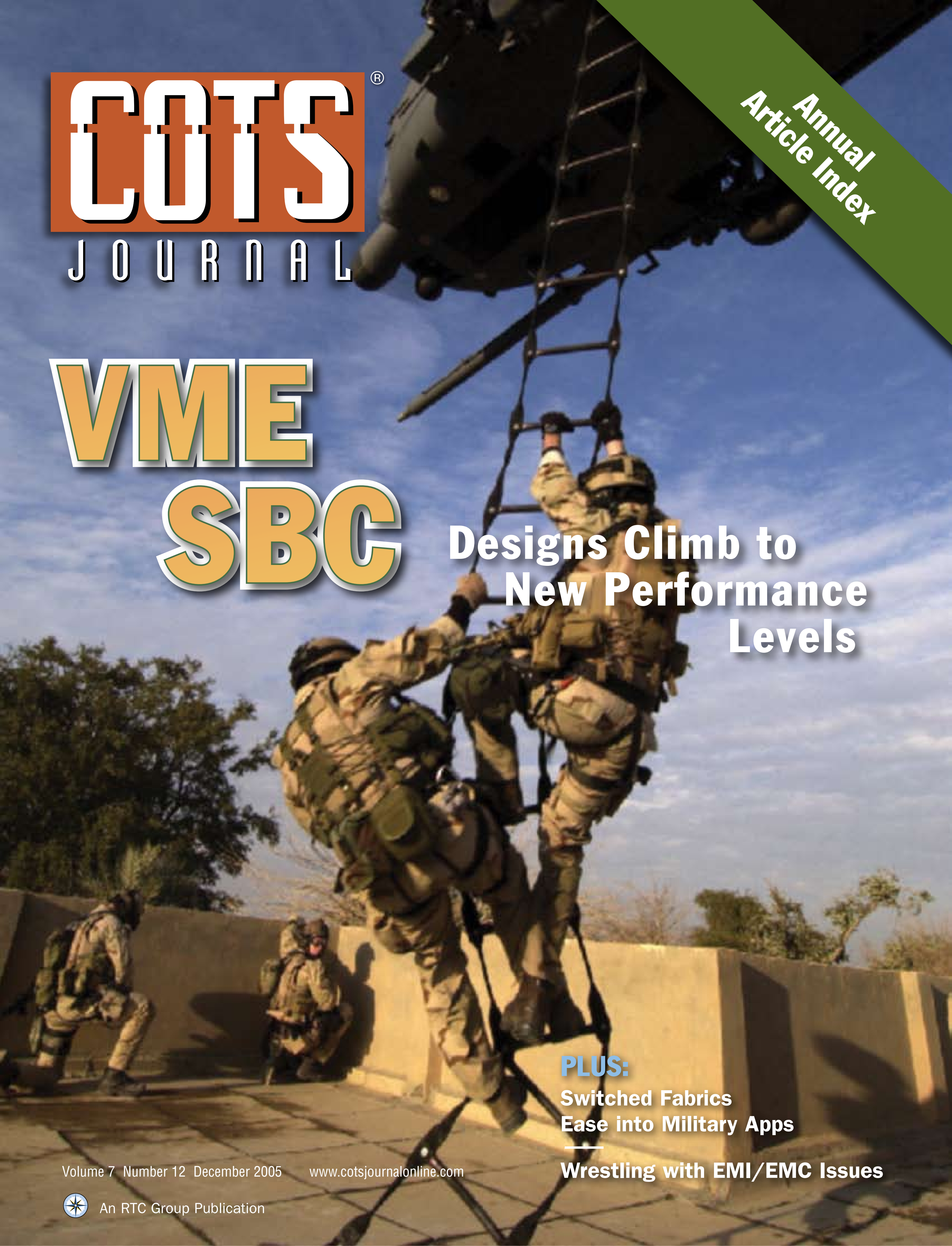


COTS® JOURNAL

Annual Article Index

VME SBC

Designs Climb to New Performance Levels

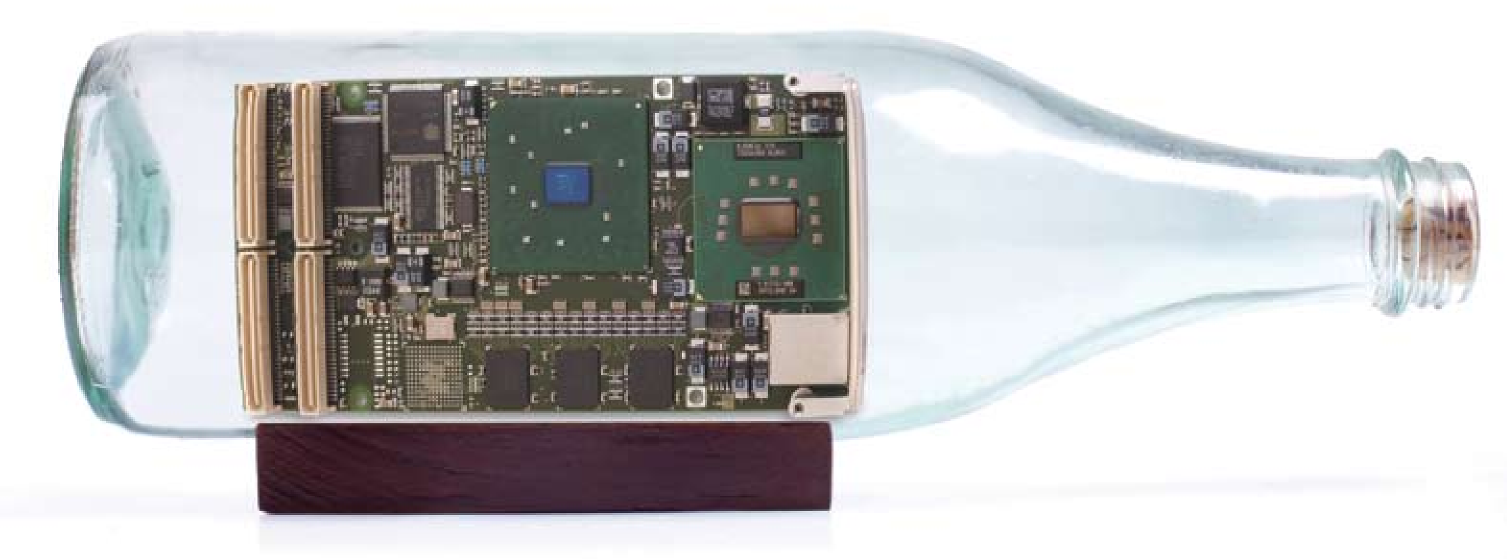
PLUS:

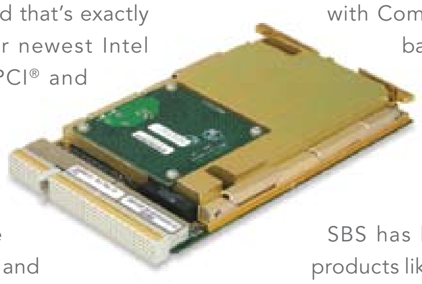
Switched Fabrics Ease into Military Apps

Wrestling with EMI/EMC Issues

Volume 7 Number 12 December 2005 www.cotsjournalonline.com

An RTC Group Publication





COTS JOURNAL

Features

December 2005 Volume 7 Number 12

Hardware Assets

VME SBCs

Tech Recon

Serial Switched Fabrics

Test & Screening

Designing for EMI/RFI

Annual Article Index

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

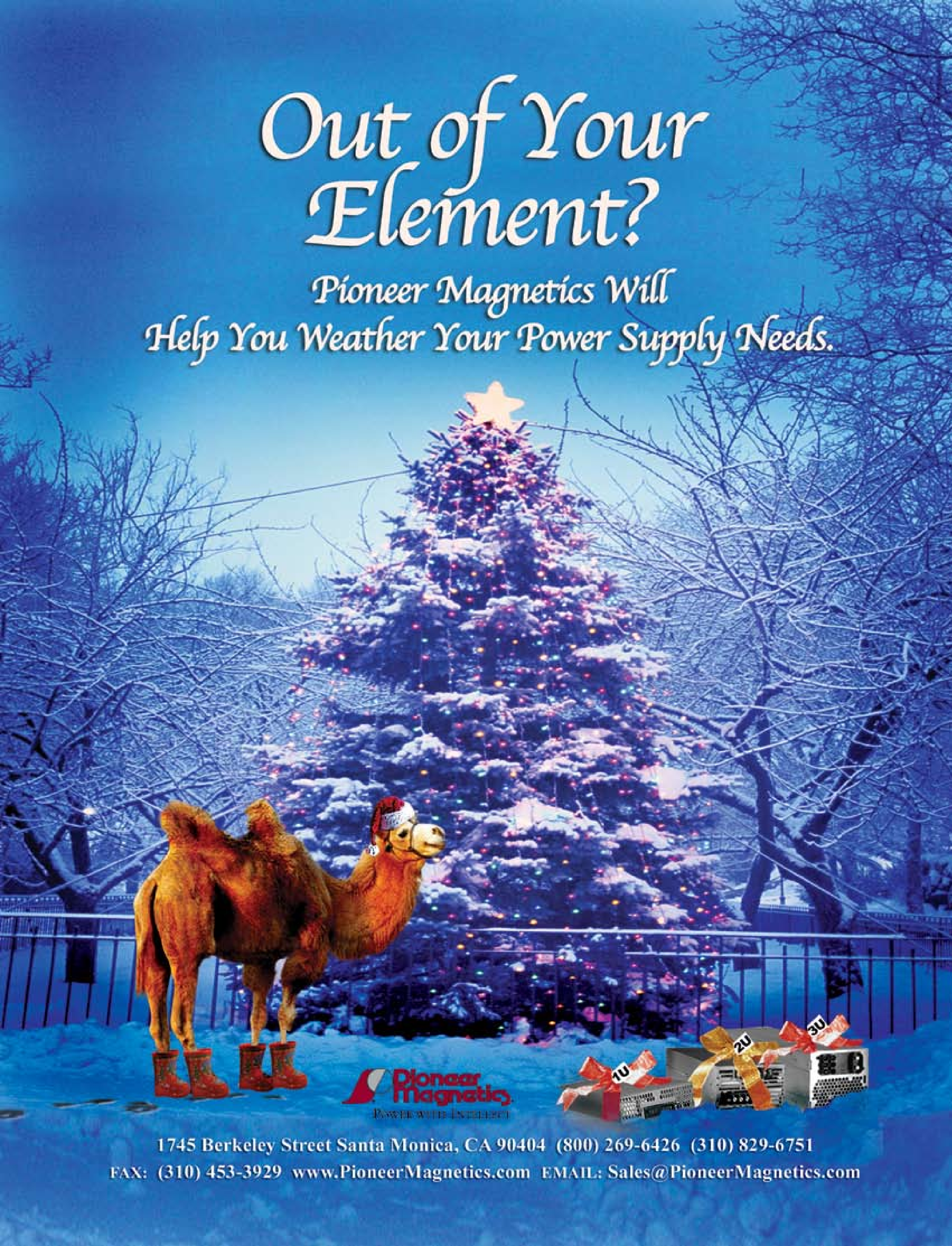
Departments

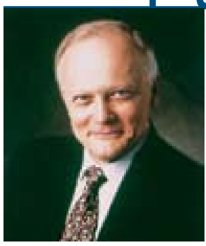
Coming in January...
...See Page 69

Cover Story.....................Page 14

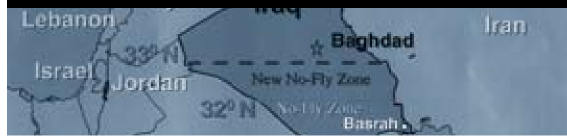
The HH-60G Pave Hawk is a highly modified version of the Army Black Hawk helicopter, which features an upgraded communications and navigation suite. The suite includes integrated inertial navigation/global positioning/Doppler navigation systems, satellite communications and secure voice communications. Shown here, Air Force pararescuemen are extracted from an abandoned housing site in Baghdad by a Pave Hawk helicopter. The Airmen are assigned to the 64th Expeditionary Rescue Squadron.

Courtesy: U.S. Air Force photo by Staff Sgt. Shane A. Cuomo


Out of Your Element?
Pioneer Magnetics Will
Help You Weather Your Power Supply Needs.
1U
2U
3U
Pioneer Magnetics
1745 Berkeley Street Santa Monica, CA 90404 (800) 269-6426 (310) 829-6751
FAX: (310) 453-3929 www.PioneerMagnetics.com EMAIL: Sales@PioneerMagnetics.com



Publisher's Notebook



An Exception? Or Is the *Rule* Wrong?

I keep hearing it over and over: the rule is conferences and shows are dead. They've been eliminated by the Internet. Lies, all lies. Conferences and trade shows are not dead, only bad conferences and trade shows are dead and they deserve to be dead. This year the I/ITSEC (Interservice/Industry Training, Simulation and Education Conference) took place earlier than in previous years, starting November 28th, enabling me to comment on it in this month's column. Members of *COTS Journal*'s editorial team have attended this conference for the last five years watching it grow every year. This year the conference organizers forecasted 500 exhibitors and 16,000 attendees making this one of the largest conferences targeting a segment of the military electronics market.

When we first started attending I/ITSEC the vast majority of the simulation and training products showcased were geared toward weapons firing and flight training. Over the years we've watched the conference's content change to include team training for tasks such as tank platoon operations and flight missions. This year we noticed that there were a significant number of exhibitions for support activities, such as cargo loading/off-loading and crane operations, and so forth. Simulation is taking over in almost every facet of the military training—wherever a simulator can be imagined one will be developed. This trend will only continue.

Given the visual reality of today's video games, it's difficult to remember that five years ago attendees at I/ITSEC were impressed by what, compared to today's simulation products, now seem very crude. At that time anyone familiar with computing could appreciate the amount of work it took to develop not only the hardware but the software for each of these systems. Those systems performed very well and achieved their goal, even though you were aware that they were simulations. In contrast, today's systems are now so elaborate that the entire experience of using these systems is almost indistinguishable from actually being out in the field (live fire excluded).

The success of I/ITSEC is not based on the supplier product offerings displayed and demonstrated on the show floor. I/ITSEC's success is based on the strength of its seminars and panels—along with a variety of topic offerings in each time slot enabling attendees to select sessions associated with their specific needs. The show floor ends up being a show-and-tell for the conference sessions, allowing attendees to touch and play with some of the toys that are available. In other words, it's a supporting element and not the primary element to the conference.

I/ITSEC isn't the exception to the rule, rather it just doesn't play in the league that says a trade show or conference is nothing but an organized sales pitch by multiple vendors. That league of conferences will clearly be eliminated by the Internet. But conferences like I/ITSEC that provide something useful to the attendees will continue to flourish. Thanks for rewriting the rule, I/ITSEC.

We're coming to the close of another year—a time when we get together with family and friends and think about how lucky we are. I never really figured out what makes this time of year so different from other times, but it is. When I greet people this time of year the handshake or the hug is tighter and longer than other times of the year. It's a time when I really get to feel how lucky I am for the people around me, and to reflect on those that are no longer a part of my life. So to each and every one of you: happy holidays and have a healthy and happy New Year; and thanks for being part of my life and letting me bore you with my opinions in *COTS Journal*. And thanks to all the men and woman who protect us and our way of life.

Pete Yeatman, Publisher
COTS Journal

U.S. Postal Service Statement of Ownership, Management and Circulation Required by 39 USC 3685.1) Title of Publication: *COTS Journal*. 2) Publication Number 1526-4653. 3) Filing Date 10/01/2005. 4) Frequency of issue is monthly. 5) Number of issues published annually: 12. 6) Annual subscription price: n/a. 7) Complete Mailing Address of Known Offices of Publication: The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673 Orange County. 8) Complete Mailing Address of Headquarters of General Office of Publisher: The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673 Orange County, California. Publisher: John Reardon, The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673 Orange County, CA 92673. Editor:Jeff Child, 20A Northwest Blvd. BMP#137, Nashua NH 03063. Managing Editor: Marina Tringali. The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673 Orange County, CA 92673. 10) Owners: James Lizzio, Jim Reardon, John Reardon, Zoltan Hunor. The RTC Group;905 Calle Amanecer, Suite 250, San Clemente, CA 92673 Orange County. 11) Known Bondholders Holding 1 Percent or More of Total Amount of Bonds, Mortgages, or Other Securities: None. 12) Tax Status: The purpose, function, and nonprofit status of this organization and the exempt status for federal income tax purposes has not changed during the preceding 12 months. 13) Publication Title: COTS Journal. 14) Issue date for Circulation data: 08/2005 COTS Journal. 15) Extent and Nature of Circulation: average number of copies each issue during preceding 12 months (Net press run): 27,051. Number copies of single issue published nearest to filing date: 30,001 a)Total number of copies (net press run). b) 1. Paid/requested outside-county mail subscriptions stated on form 3541. (Include advertiser's proof and exchange copies)/Average number copies each issue during preceding 12 months: 29,023, number copies of single issue published nearest to filing date: 30,001. b)2. Paid in-county subscriptions (include advertiser's proof and exchange copies)/average number copies each issue during preceding 12 months/number copies of single issue published nearest to filing date: n/a. b)3. Sales through dealers and carriers, street vendors, counter sales and other non-USPS paid distribution/average number copies each issue during preceding 12 months: n/a, number copies of single issue published nearest to filing date: n/a. b)4. Other classes mailed through the USPS/average number copies each issue during preceding 12 months: n/a, number copies of single issue published nearest to filing date: n/a. c) Total paid and/or requested circulation [sum of 15b. (1), (2), (3) and (4)]/ average number copies each issue during preceding 12 months: 27,051, number copies of single issue published nearest to filing date: 29,023. d) Free distribution outside of the mail (carriers or other means)/ average number copies each issue during preceding 12 months :n/a number copies of single issue published nearest to filing date: n/a. f) Total free distribution (sum of 15d. and 15e.)/ average number copies each issue during preceding 12 months: 1,335, number copies of single issue published nearest to filing date: 939. g) Total distribution (sum of 15c and 15e)/ average number copies each issue during preceding 12 months: 26,960 number copies of single issue published nearest to filing date: 29,959. h) Copies not distributed/ average number copies each issue during preceding 12 months:91 , number copies of single issue published nearest to filing date: 39. I) Total (sum of 15g and h)/ average number copies each issue during preceding 12 months: 27,051, number copies of single issue published nearest to filing date: 30,001. j) Percent paid and/or requested circulation (15c divided by 15g times 100)/ average number copies each issue during preceding 12 months: 98.71, number copies of single issue published nearest to filing date: 95.31. 16. Publication of statement of ownership. Publication will be printed in December issue of this publication. 17) Signature and title of the editor, publisher, business manager or owner: Marina Tringali (Managing Editor), Date: 10/01/2005.

I certify that all information furnished on this form is true and complete. I understand that anyone who furnishes false or misleading information on this form or who omits material or information requested on the form may be subjected to criminal sanctions (including fines and imprisonment)and/or civil sanctions(including multiple damages and civil penalties).

Publisher

PRESIDENT
John Reardon, johnr@rtcgroup.com

PUBLISHER
Pete Yeatman, mail@yeatmangroup.com

EDITORIAL DIRECTOR / Associate Publisher
Warren Andrews, warrena@rtcgroup.com

Editorial

EDITOR-IN-CHIEF
Jeff Child, jeffc@rtcgroup.com

SENIOR EDITOR
Ann Thryft, annt@rtcgroup.com

CONTRIBUTING EDITOR
David Cotton, davidc@rtcgroup.com

MANAGING EDITOR
Marina Tringali, marinat@rtcgroup.com

STAFF EDITOR
Craig Choisser, craigc@rtcgroup.com

COPY EDITOR
Rochelle Cohn

Art/Production

CREATIVE DIRECTOR
Jenna Hazlett, jennah@rtcgroup.com

DESIGNER
Melissa Gaeta, melissag@rtcgroup.com

PRODUCTION DESIGNER
Kirsten Wyatt, kirstenw@rtcgroup.com

DIRECTOR OF WEB DEVELOPMENT
Jan Garcia, jang@rtcgroup.com

WEB DEVELOPER
Marke Hallowell, markeh@rtcgroup.com

Advertising

CALIFORNIA COASTAL ADVERTISING MANAGER
Diana Duke, dianad@rtcgroup.com
(949) 226-2011

WESTERN REGIONAL ADVERTISING MANAGER
Lea Ramirez, lear@rtcgroup.com
(949) 226-2026

EASTERN REGIONAL ADVERTISING MANAGER
Nancy Vanderslice, nancyv@rtcgroup.com
(978) 443-2402

EMEA SALES MANAGER
Anna Brown, annab@rtcgroup.com
(949) 226-2025

BUSINESS DEVELOPMENT MANAGER
John Koon, johnk@rtcgroup.com
(858) 755-4999

BILLING
Maggie McAuley, maggiem@rtcgroup.com
(949) 226-2024

COTS Journal

HOME OFFICE

The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673
Phone: (949) 226-2000 Fax: (949) 226-2050, www.rtcgroup.com

EDITORIAL OFFICES
Warren Andrews, Editorial Director/Associate Publisher
39 Southport Cove, Bonita, FL 34134
Phone: (239) 992-4537 Fax: (239) 992-2396

Jeff Child, Editor-in-Chief
20A Northwest Blvd., PMB#137, Nashua, NH 03063
Phone: (603) 429-8301 Fax: (603) 424-8122

Ann Thryft, Senior Editor
15520 Big Basin Way, Boulder Creek, CA 95006
Phone: (831) 338-8228

Published by THE RTC GROUP

ROCKET SCIENCE AT ROCKET SPEED.

At 2 GHz, it's not just fast. It's simply brilliant!

Blast off with the new Model 6826 A/D board. It's fully loaded with dual 2 GHz 10-bit A/D converters, powerful FPGA resources, plenty of memory and fast interfaces—all ready to tackle your toughest high-speed wideband signal processing tasks.

Capture. Digitize both continuous or burst signals and pulses with flexible clocking, gating and triggering resources plus advanced multiboard synchronization. Store real-time data in dual 512 MB DDR memory buffers.

Crunch. Process real-time data in the Xilinx XC2VP100 Virtex-II Pro FPGA with nearly 100,000 logic cells and 444 hardware multipliers—perfect for DSP algorithms.

Connect. Stream data through FPDP-II or VXS using Serial RapidIO, PCI Express, or Aurora and 3.125 Gbit/sec RocketIO® gigabit serial interfaces.

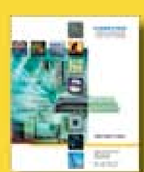
The 6826 is the latest VME addition to over 60 Pentek I/O products. From stand-alone VME/VXS, PMC/XMC, cPCI or PCI boards to application-ready solutions, Pentek offers you lifetime technical support and a priceless extra: the power to outrun, outsmart and out-process your competitors!

- Dual 10-bit 2 GHz A/D Converters
- Dual 4x Full-Duplex VXS Links
- Xilinx Virtex-II Pro XC2VP100 FPGA
- 1 GByte of DDR SDRAM
- FPDP-II, LVDS, VXS, Aurora®, Serial RapidIO, & PCI Express
- Multiboard Synchronization, Gating & Triggering
- ReadyFlow® Board Support C Libraries
- SystemFlow™ API & Libraries
- GateFlow® FPGA Design Resources
- Commercial, Rugged & Conduction-Cooled Versions

Also check out our RTS2503 Wideband Recording System. Complete with SystemFlow API and Development Libraries!

PENTEK

www.pentek.com/go/cotsrocket for Pentek's "*Critical Techniques for High-Speed A/D Converters in Real-Time Systems*" handbook and to request a full product catalog.



Pentek, Inc., One Park Way, Upper Saddle River, NJ 07458 Phone: 201.818.5900 Fax: 201.818.5904 e-mail:info@pentek.com www.pentek.com
Worldwide Distribution and Support

The Inside Track

Army Awards $42.4 Million Contract for Net-Centric Comms Gear

The U.S. Army Communications-Electronics Command in Fort Monmouth, NJ has awarded DataPath a $42.4 million firm-fixed-price contract for custom satellite earth terminals and associated services. This award extends the Army's Joint Network Node (JNN) initiative to provide enhanced communications services to multiple National Guard Units in Iraq and provides additional capabilities to the Marine Corps' Video Storage Wide Area Network (VSWAN) and Logistics Support Wide Area Network (LSWAN) initiatives.

Under the terms of the contract, DataPath will deliver DataPath ET 3000 Portable trailer-based satellite earth terminals and DataPath DKET 5000 Transportable self-contained satellite earth terminals. DataPath will also provide the Army with associated integrated logistics and depot support as well as technical and engineering support.

Deployed extensively in Iraq, the JNN initiative is a network-centric communications architecture, which currently provides portable communications to the U.S. Army Third Infantry Division, 101st Airborne Division, Fourth Infantry Division and 10th Mountain Division. DataPath recently announced a $96 million contract for additional JNN deployments to the First Cavalry Division, the 25th Infantry Division, the 82nd Airborne Division and multiple Army National Guard units.

Datapath
Duluth, GA.
(678) 597-0300.
[www.datapath.com].

Figure 1

The DataPath 3000 is a compact trailer-based satellite earth terminal that delivers a tactical, rugged communications gateway to battalions for Communications On The Quick Halt (COTQH).

Isonics and Bell Labs Team to Develop Military Night Vision Systems

Isonics and Lucent Technologies Bell Labs announced today that they have entered into a development agreement to create a next-generation infrared imaging and night vision surveillance technology based on pioneering research by Bell Labs at its micro electro-mechanical systems (MEMS) and nanotechnology fabrication facility. The development plan contemplates a proof-of-concept within 12 months, followed by steps toward commercialization.

Infrared technology, which converts infrared radiation in the non-visible spectrum, such as body heat, into a visible image, is commonly found in both commercial and military/homeland security applications including night vision goggles and cameras, rifle scopes and threat detection devices used to identify concealed weapons or explosives.

The agreement calls for cross-licensing of relevant Isonics and Bell Labs intellectual property and for Isonics to contribute to the development costs during the three-year development phase. Isonics receives exclusive rights to newly created technical information for MEMS-based IR imaging modules except for certain rights reserved by Lucent. Lucent will manufacture test structures and prototypes and has the right to manufacture commercial IR imaging modules for sale to Isonics. Isonics may incorporate these modules into IR cameras and systems it develops internally or through collaborations with others in the industry.

Isonics
Golden, CO.
(303) 279-7900.
[www.isonics.com].

Lucent Technologies
Murray Hill, NJ.
(908) 582-3000.
[www.lucent.com].

Curtiss-Wright Earns AS9100 Certification

Curtiss-Wright Controls Embedded Computing has been awarded AS9100 certification for its Leesburg, Virginia and Ottawa, Ontario operations. AS9100, which is overseen by the International Aerospace Quality Group, standardizes quality management system requirements and delivers quality assurance in design, development, production, installation and servicing. The standard also drives cost reductions throughout the aerospace industry supply chain. Curtiss-Wright's accreditation program was directed by Gerry Bellehumeur, Quality Director, Curtiss-Wright Controls Embedded Computing, Ottawa. The AS9100 audit was performed by TUV America.

Meeting AS9100 has become an increasingly important milestone for embedded computing suppliers of aerospace systems and components. Increasingly, major aerospace contractors are requiring AS9100 compliance. Suppliers to Boeing, for example, must meet requirements for the Boeing Quality Management System (BQMS), which includes AS9100 certification, or they must be granted a special waiver. The benefit for leading aerospace contractors and their customers is significantly improved product quality and associated reduction in costs. AS9100 compliance exceeds the ISO9001:2000 quality standard, on which it's based, with additional quality system

requirements such as independent validation of materials and processes. It adds approximately 80 additional requirements and 18 amplifications to the ISO 9001:2000 standard. The standard addresses the unique, complex and highly regulated nature of the defense aerospace industry.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

New Industry Standards Forum Targets Multi-Core Processor Issues

A new industry group aims to provide a neutral forum where vendors in the multiple-core processor space can work out standards for interprocessor communications, debug, and other common technology hurdles in multicore implementations. Being organized as The Multicore Association, the new group is an outgrowth of meetings among chip vendors, semiconductor IP providers, as well as RTOS, compiler and development-tool vendors, which have been ongoing since May. Its focus will be on nonproprietary implementations where products from multiple vendors must work together. The group has set its initial focus on multitasking and communications application program interfaces (APIs) and debug, with the goal of eventually providing a forum in which all relevant embedded multicore standardization issues can be discussed and resolved.

Leading the effort is Markus Levy, a well-known processor analyst who also founded and is president of EEMBC, the Embedded Microprocessor Benchmark Consortium. Levy defines the scope of The Multicore Association's domain as implementations that use two or more processing elements. These include, but are not limited to, heterogeneous and homogeneous multiprocessor systems, coprocessors and hardware accelerators.

Figure 2

Shown here launching decoys, the Airbus A400M airlifter was conceived to fit the needs of eight European Air Forces for a new generation military airlifter. The aircraft boasts fly-by-wire flight control system with sidestick controllers. The aircraft will first fly in 2008 with deliveries beginning in 2009. Image courtesy of: Airbus Military

The Multicore Association
Eldorado Hills, CA.
(530) 672-9113.
[www.multicore-association.org].

Aviatronics Chooses Concurrent's Linux for Airbus A400M Aircraft

German consortium Aviatronics has selected Concurrent's iHawk powered by RedHawk Real-Time Linux for the Airbus A400M military transport aircraft. Concurrent's hardware-in-the-loop (HIL) system will be used to test the aircraft's high-lift control computers, which are responsible for controlling the trailing-edge flaps that generate higher lift during take-off and landing.

To simulate aircraft behavior and record test data, the HIL system will use two iHawk 4-CPU and 2-CPU real-time computers. HIL simulation is a critical product development process providing comprehensive testing of components in a virtual environment in which other subsystems are replaced by mathematical models. Components to be tested are inserted into a closed loop that is reproducible, systematic, fast and more reliable than actual bench testing. Concurrent's iHawk systems are powered by up to eight Intel Xeon or AMD Opteron processors and up to 64 Gbytes of memory in rackmount and tower enclosures. iHawks are true symmetric multiprocessors that run a single copy of RedHawk Linux.

Concurrent
Duluth, GA.
(678) 258-4000.
[www.ccur.com].

VITA 55 Spec Offers Alternative to Switched Fabrics

Under development by the VITA Standards Association (VSO), a new specification, dubbed the Virtual Streaming Protocol (VSP) or VITA 55, is targeting data communications within high-performance embedded systems. The spec is intended to provide more processing power for image or signal processing applications without the overhead of general-purpose switched fabric solutions. VSP is based on the combination of board-to-board interconnect standards such as VITA 41 (VXS) and VITA 42 (XMC), and existing FPGA-based link layer solutions such as Xilinx's Aurora interface. VSP combines specific link layer interfaces with a transport layer targeted at applications that need basic transport services at minimum cost in FPGA resources.

The VITA 55 standard is being developed within the VITA Standards Organization (VSO), an ANSI-accredited standards body within the VMEbus Industrial Trade Association (VITA). The VITA 55 task group was co-sponsored by TEK Microsystems, Inc, QinetiQ and Mercury Computer Systems and has active participation from many other companies in the high-performance embedded marketplace, including Curtiss-Wright Controls Embedded Computing, Pentek and VMETRO.

The VITA 55 standard is currently in draft development and is expected to move to initial ballot review in the spring of 2006. Products based on VITA 55 are expected to reach the market during the same time period. Because VITA 55-compatible products are by definition based on reconfigurable FPGA technology, products can be updated to support revisions to the standard through FPGA upgrades without hardware changes.

TEK Microsystems
Chelmsford, MA.
(978) 244.9200.
[www.tekmicro.com].

COTS Websites

www.vita.com

VITA Web Site Serves Up More Than Just VME

Because VME is so entrenched among military system designers, there are probably only a scant few of *COTS Journal* readers that are unfamiliar with the VMEbus International Trade Association, or VITA, as it's more commonly known. That said, anyone who hasn't visited the VITA Web site in a while may find it worth checking out. Aside from its exemplary job as the key portal for the VITA Standards Organization (VSO) activities, VME specs and everything else VME-related, the site provides a rich assortment of product directories—VME, PCI and mezzanines—and details on VITA-sponsored events such as the Bus&Board conference and the more recent

Military Embedded Electronics & Computing Conference (MEECC)—a technical conference for uniformed and non-uniformed persons engaged in the design, development, deployment and support of electronics and computers for the military.

For its part, the VSO is accredited as an American National Standards developer and a submitter of Industry Trade Agreements to the IEC. The VSO has created more than 30 standards in the past 10 years that promote open technology systems. Registered members can download the minutes of past VSO meetings and the various presentations given at those meetings. The VITA site now even has a market overview section, with detailed graphical roadmaps of where VME technology is headed and a breakdown of the various application areas. Links to articles about VME are also provided.

VMEbus International Trade Association, Fountain Hills, AZ. (480) 837-7486. [www.vita.com].

VME SBC Designs Wrestle with Fabrics, I/O Issues

VME single board computer developers continue to churn out innovative designs targeted for military use. Integrating switched fabrics and other serial I/O schemes top the list of next-gen challenges.

Jeff Child

Still holding a firm grip on its position as the leading embedded board form-factor in the military market, VME boasts a longevity few bus standards can claim. Although approaching its quarter-century birthday (next year), VME has lost little momentum as the leading form-factor in the military/COTS industry. It's keeping ahead of the performance curve by riding the wave of the various switched fabric schemes such as InfiniBand, Serial RapidIO, Gbit Ethernet, PCI Express and the Xilinx Aurora fabric.

As these get rolled into VME standards such as VITA 41, VITA 42, VITA 46, VITA 56 and others, efforts remain to keep VME as compatible as possible with previous generation boards, backplanes and boxes. The adoption of switched fabrics in fact ranks as the more significant technology trend shaping the design of today's crop of VME single board computers (SBCs), according to a

InfiniBand Technology Connects Onboard

Dave Wessing, Vice President and General Manager, Government Group
SBS Technologies

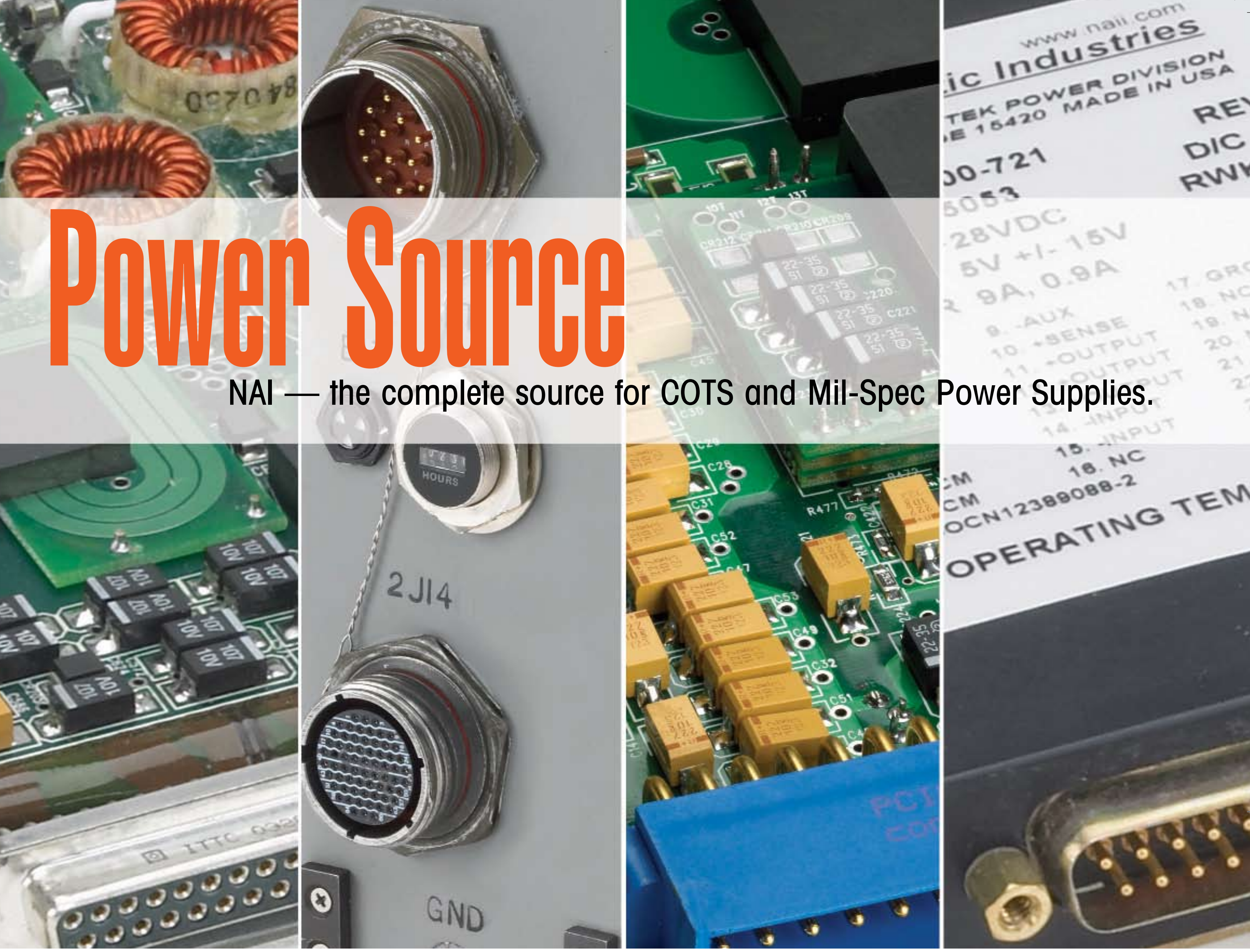
The U.S. Navy faces many of the same communications requirements that face commercial enterprises, like support for voice, data, video and imaging as well as security and Quality of Service (QoS) guarantees of how various communications get prioritized on the network.

Although various commercial-grade components and technologies are being used by shipboard systems today, commercial-grade solutions can pose some disadvantages if the Navy's stringent requirements for survivability are not met. In addition to reliable system operation, other mission-critical networking requirements for the Navy fleet include:

- High-performance, low-latency throughput from application to application across the network infrastructure;
- Security, which includes the protection of classified data through encryption, filtering, access and login control, among other techniques;
- Scalability, which implies the ability to add bandwidth between end systems or between components of the network infrastructure, and the ability to add additional end systems or components.

InfiniBand technology, which has been marketed heavily for use in IT departments for enterprise servers, is well suited to meet the Navy's requirements for performance, scalability, redundancy, QoS and more. InfiniBand is a unified network technology that encompasses the local bus architectures (such as PCI) that are the primary pathways between the CPU, memory and peripheral devices. It also includes standard industrial buses like VME that connect to an intelligent or non-intelligent backplane, primarily used for industrial, telecommunications and military applications, and Local Area Network (LAN) bus architectures, such as Fibre Channel and Gbit Ethernet.

The most obvious benefit of InfiniBand technology is bandwidth. InfiniBand provides 10 Gbit/s performance with ease, and PCI Express hardware-based platforms deliver greater than 2 Gbytes/s. Dual Data Rate and Quad Data Rate InfiniBand implementations will deliver 120 Gbits/s well ahead of any other technology and can provide the U.S. Navy with significant headroom for growth above and beyond Ethernet.



An equally important parameter is latency—the amount of time it takes for a packet to go from one end of a network to the other. A well-designed packet switch is critical to low latency, and InfiniBand technology was designed so that a switch can cut through a packet from input port to output port before the packet has even fully arrived. Other switch architectures incur higher latencies by requiring an entire packet to be fully buffered before routing decisions are made.

Reliable network systems are critical to a ship's mission and the lives of its sailors. Because reliability has been "designed-in," InfiniBand technology's inherent fault tolerance allows individual components to be repaired, upgraded or replaced without bringing the network fabric and its applications down. Most of the components are hot plug-able, so if a component fails, it can be swapped out without powering down the chassis. InfiniBand switches and nodes can be configured with redundant paths between end nodes, and end nodes can also have multiple ports. And if a given path becomes unusable, the hardware can failover to an alternate path/port.

Dependable InfiniBand technology provides the U.S. Navy with an open architecture, high-performance, fault-tolerant network technology that can serve as a unifying network interconnect for all systems and nodes on a ship's network. Security, performance and scalability make InfiniBand technology ideal for the U.S. Navy's networking requirements in today's complex ships.

SBS Technologies
Albuquerque, NM.
(505) 875-0600.
[www.sbs.com].

recent survey *COTS Journal* conducted of VME SBC vendors. Aside from fabrics, vendors that responded to the survey also cited multicore processors, increasing I/O demands and cooling as the key challenges they're wrestling with.

Fabrics on VME

The VME community has been busy over the past couple of years crafting a number of specs that incorporate switched fabrics. Among those currently under development are VITA 41, VITA 42 and VITA 46. VITA 41 (VME Switched Serial or VXS) is an evolutionary draft standard that enhances the existing parallel VMEbus to support switched fabrics while maintaining backward compatibility with existing VME backplanes. VITA 42 (Switched Mezzanine Card or XMC) is an evolutionary draft standard that adds

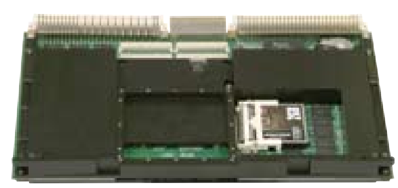


Figure 1

A lot of advanced I/O functionality can be leveraged from the x86 laptop realm. Dynatem's RPM design does just that, sporting a low-power Pentium M processor. The 855GME Graphics Memory Controller Hub (GMCH) and 6300ESB I/O Controller Hub (ICH) chipsets support PCI-X expansion, integrated VGA/DVO interface, USB 2.0, ATA/100 and Serial ATA (SATA). Two USB 2.0 ports, a COM port and IDE are all accessible from the rear P2 connector. SVGA and Digital Video Output (DVO), dual 10/100/1000BaseT (VITA 31.1-compatible), dual SATA and LPC bus are routed to the optional P0 connector. Onboard CompactFlash permits single-slot booting. One PMC-X site is provided for additional I/O expansion.

high-speed interfaces to existing PMC mezzanines to support multiple high-speed fabrics while retaining compatibility with existing PMC sites. Meanwhile, another spec, VITA 46, promises a more revolutionary upgrade to military subsystem architectures with high-speed switched serial backplanes that support Advanced Switching Interconnect (ASI) and Serial RapidIO. For a look at how fabric implementations in the VME realm contrast to those in telecom designs, see the sidebar "VME's Tipping Point" on p.18 within this article.

On the fabric front, most vendors surveyed agree that PCI Express is the switched fabric that will dominate the I/O space. PCI Express is expected to dominate because it has tremendous scalability, and it will be ubiquitous since it will be the standard for chip-level interconnect. And Advanced Switching Interconnect (ASI) was also viewed by some as the most compatible with PCI Express. Before Advanced Switching technology gains traction, many cite switched Gbit Ethernet as the "here today" choice.

For peer-to-peer interconnects, Serial RapidIO and Advanced Switching Interconnect each seem to have a fit in the market. For its part, Curtiss-Wright Controls Embedded Computing (CWCEC) says its multi-computing interconnect strategy is to offer InterProcessor Communications (IPC) software that enables customers to abstract from the fabric standard and enable technology progression over time, independent of the fabric choice. Emerging VITA specs, like the VITA 46 standard, define a core fabric connectivity that can accommodate any of these fabric choices, either in a centralized or distributed switching architecture. Meanwhile, SBS Technologies is among the strongest proponents of the InfiniBand switched fabric technology. For more on InfiniBand as a solution for naval computing needs, see the sidebar "InfiniBand Technology Connects Onboard" on p.14 within this article.

Trends in I/O

The military's move toward network-centric warfare and associated ramp-ups in sensor processing, data acquisition and image capture and analysis make today's applications particularly demanding in their I/O requirements. The VME SBCs of the future will need to deliver flexible, cost-effective I/O functionality through innovations such as the use of FPGA technology or add-on daughter modules.

Just as today's range of switched fabric technologies are serial, so are many of the other I/O functions in embedded computers. Fortunately a lot of the silicon

VME's Tipping Point

Ray Alderman, Executive Director
VMEbus International Trade Association

It's no secret that we're now in the middle of tremendous technological change and turmoil today. Buses have reached their performance limits, and everyone seems to be enchanted with high-speed serial fabrics as the next great computing interconnect. But, switched fabrics can't do what buses like VME can do, especially in deterministic applications. And fabrics have a lot of warts on them; computer science problems that pop up in networked architectures, which can enslave embedded software writers for years.

At this juncture, switched fabrics are a bit of a technological novelty, and such novelties always target the easiest and least-demanding applications first. Take telecom for example. QoS (Quality of Service) in telecom is NOT a critical application. That's why your calls are dropped, you don't get a dial tone when you pick up your phone and you don't get any "bars" on your cell phone. The only critical application in telecom is QoB (Quality of Billing). You'll never get more minutes on your calling plan than you contracted for, and you won't ever make a single long-distance call for free. Some fabrics, especially cheap commodity fabric technologies, will find ready acceptance in the edge equipment handling calls and packets, but they are not yet robust enough to handle the billing systems.

Besides, all telecom gear sits in a central office, a benign environment that's perfectly air-conditioned, and it doesn't have to endure dust, dirt, shock, vibration, temperature extremes, oil, grease, explosions or chemical contaminants. That's why the VITA 41 and VITA 46 fabric architecture specifications concentrate on making fabrics operate in such harsh environments.

VITA has been the crucible of rugged computer specifications for the past 25 years. Everything that goes into our specifications ensures that even commodity fabric silicon can survive the tough environments found in MIL/COTS and high-end industrial applications. There are no other specifications in the world that have so many survivability, cooling and ruggedization mechanisms in the document.

Adding fabric connections to VME, as we have done in VITA 41, gives designers of harsh-environment systems a starting point for deploying reliable and survivable implementations of the fabrics. VITA 46 allows designers of embedded supercomputers in MIL/COTS applications to design and deploy more computing power than what many of the world's super minicomputers touted just a few years ago. And both architectures can handle the tremendous shock, vibration, temperature extremes and contaminants that none of the commercial or telecom computers could survive for more than a few minutes.

As we go forward, the ruggedness and robustness of the latest VITA fabric specifications will give designers the ability to use an open standard, along with readily available and interoperable products, to build some of the toughest and most reliable computers that can survive the world's most threatening and destructive environments. That is what the new VITA fabric specifications are all about.

VMEbus International Trade Association (VITA)
Fountain Hills, AZ.
(480) 837-7486.
[www.vita.com].

for those functions—many of which are serial—can be leveraged from the laptop market. This includes USB 2.0, graphics, SATA, IDE, Gbit Ethernet and bootable CompactFlash. With PMC sites taking up valuable front panel space and rear I/O pins, the one technology challenge is providing as many I/O routing options as possible, especially rear I/O.

An example of a VME making full use of processor and I/O technology developed for the PC laptop is Dynatem's RPM (Figure 1), a rugged conduction-cooled VMEbus- (and VME64)-compatible platform based on the Intel low-power Pentium M (Dothan) processor. The 855GME Graphics Memory Controller Hub (GMCH) and 6300ESB I/O Controller Hub (ICH) chipsets support PCI-X expansion, integrated VGA/DVO interface, USB 2.0, ATA/100 and Serial ATA (SATA). Two USB 2.0 ports, a COM port and IDE are all accessible from the rear P2 connector. SVGA and Digital Video Output (DVO), dual 10/100/1000BaseT (VITA 31.1-compatible), dual SATA and LPC bus are routed to the optional P0 connector. Onboard CompactFlash permits single-slot booting. One PMC-X site is provided for additional I/O expansion.

The RPM is the same board design as the convection-cooled DPM. The DPM typically uses front-panel I/O routing but can be provided with identical I/O routing as the RPM for application development in a standard VMEbus chassis.

Backward Compatibility

At the same time that all these expanded features are being required, a large number of the installed VME customer base is tied to three slot row backplanes with 5V-only power. This requirement combined with demands for ever higher performance requires a key

Company	Model Number	Processor(s)	PMC Sites	Onboard I/O & Interfaces	Special Features	Price	Intro Date
ACTIS Computer	VSBC-6872	Motorola MPC8270	1	2 S-ATA hard disk, 3 fast Ethernet, 1 RS-232, 4 RS-232 or RS422/485/ V.35	PowerQUICC II; CompactFlash	$2,083.33	Sep 2004
Aitech Defense Systems	C106	Motorola PowerPC G4+ MPC7447A	2	3 fast Ethernet, 2 dual-redundant MIL-STD-1553B, 2 USB 2.0, 10 standard serial, discrete I/O	3 ruggedization levels; 64-bit, 66 MHz PCI bus; flash	Starts at $6,400	Mar 2005
American ELTEC	BAB 760	PowerPC 750 GX or FX	1-2	Through PMC modules	PCI architecture in combination with FPGA-based VME interface	$3,995	Mar 2005
Concurrent Technologies	VP 307	Pentium M processor 760	1-3	2 Gbit Ethernet, graphics, RS232/422/485, USB, EIDE	VITA 31.1 support; 32 Mbytes of flash for applications	Starts at $4,250	Feb 2005
Curtiss-Wright Controls Embedded Computing	PMA	Ultra Low Voltage (1.0 GHz @ 5W) or Low Voltage (1.4 GHz @ 10W) Pentium M processor	1 PMC-X	ATA/100 & Serial ATA data storage, DVI-I, 2 USB 2.0, 10/100BaseTX, COM	64-bit/66 MHz PCI-X data bus	Starts at $6,433	2005
DNA Computing Solutions	Nexus	Motorola 7447/A PowerPC	2 PMC-X	Gbit Ethernet, serial	2eSST PCI-X-to-VME bridge; VME master or slave	$6,995 in quantity	Jan 2005
Dynatem	RPM	Pentium M processor	1	EIDE port, 2 Serial ATA, 2 Gbit Ethernet, DVO/VGA, high-performance graphics 2 USB 2.0, COM (RS-232/422/485)	PCI-VMEbus interface; CompactFlash	$6,700 in single quantity	May 2005
GE Fanuc	VMIVME-7807	Pentium M processor	1 PMC-X	2 10/100BaseT Ethernet, 4 USB 2.0, SVGA, 4 serial, Serial ATA, IDE and DVI	VITA 31.1 support; CompactFlash	Starts at $3,895	Sep 2004
General Micro	V169-FPIO	Pentium M or Low Voltage (LV) Pentium M-738	3	2 high-resolution video displays; 2 Gbit Ethernet, 2 Ultra SCSI-320, 4 USB	CompactFlash	Starts at $3,795	May 2005
Kontron Modular (PEP)	VMP3	Freescale MPC8541 PowerPC	1-2 via VMP1-IO modules	Fast Ethernet, 2 Gigabit Ethernet, serial	PowerQUICC III RISC processor; PCI-X to VMEbus bridge; integrated security engine; flash optional	OEM starts at $1,295; E/U starts at $1,995	Feb 2005
Motorola Computer	MVME3100	Freescale MPC8540 PowerPC	2 PMC-X	Gbit Ethernet, serial, USB 2.0, SATA	PCI-X to VMEbus bridge; VME64 and 2eSST protocols	From $1,800 to $2,400	Jan 2005
Radstone Technology	PPC7D	Freescale 1.13 GHz 7447A PowerPC processor	2	Either dual channel, dual redundant MIL-STD-1553 or integrated graphics accelerator plus 8- or 16-bit Ultra SCSI capability (via AFIX)	AFIX (Additional Flexible Interface Xtension) site; 5 ruggedization levels	OEM starts around $6,000	July 2004
SBS Technologies	VXS1	Freescale MPC7447A G4 PowerPC	1	2 Gbit Ethernet, 2 Multi-Protocol Serial Controller (MPSC)	VITA 41-based, InfiniBand-enabled; VME 2eSST protocol; extended temperature range	$5,800	Jan 2005
Thales Computers	PENTXM	1.6 GHz Pentium M or 1.8 GHz Pentium M 745 processor	2	2 10/100/1000 Ethernet, graphics, onboard hard disk drive option	Rugged version; CompactFlash or IBM/Hitachi MicroDrive	E/U starts at $4,188	May 2005
Themis Computer	PPC64	IBM PowerPC 970FX-based single and dual processor versions	7 via VME PCI carrier cards	10/100 Ethernet, 2 Gbit Ethernet, 2 Ultra320 SCSI, 6 USB and 2 serial	Dual processor Symmetric Multiprocessing (SMP) configuration	OEM $5,495 to $10,325	Feb 2005

Table 1

Listed here is a selection of fifteen VME SBC products introduced within the past year.

Many of the VME SBC board vendors surveyed said boards with multicore processors will be part of their VME SBC roadmaps.

focus on minimizing power consumption, and efficient thermal design. The requirement of many military customers for expanded operating temperatures and high shock/vibration immunity makes the thermal challenge even greater.

Many of the VME SBC board vendors surveyed said boards with multicore processors will be part of their VME SBC roadmaps. Driving that need are demands to get as much functionality as possible on a single board. That means dealing with an increase in I/O pin counts in addition to the related power issues. A number of vendors selected dual Freescale 7448s as exemplifying that trend, with a planned migration to multicore processors such as the Freescale 8641 in the near term. For a snapshot of example VME SBCs introduced within the past year, see Table 1. For an expanded analysis and details on those products see the Tech Focus section on VME SBCs starting on p.56 of the July 2005 issue of *COTS Journal.*

ACTIS Computers
Tempe, AZ.
(480) 838-1799.
[www.actis-computer.com].

Aitech Defense Systems
Chatsworth, CA.
(888) 248-3248.
[www.rugged.com].

American ELTEC
Las Vegas, NV.
(702) 878-4085.
[www.americaneltec.com].

Concurrent Technologies
Ann Arbor, MI.
(734) 971-6309.
[www.gocct.com].

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

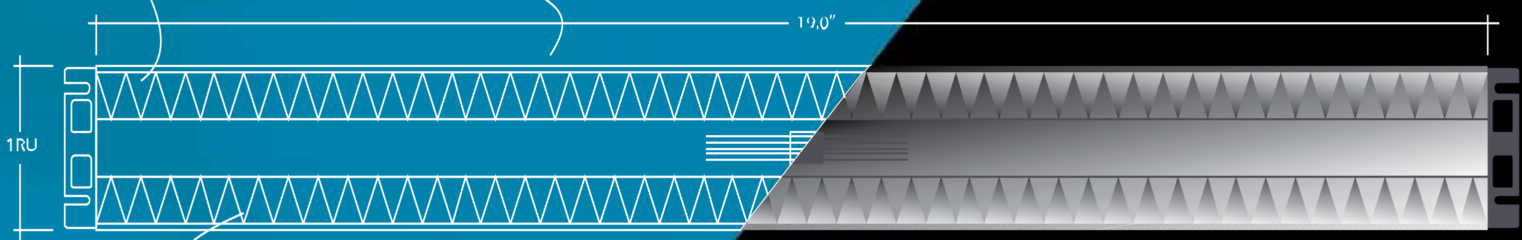
DNA Computing Solutions
Richardson, TX.
(972) 671-1972.
[www.dna-cs.com].

Cool. Calm. Collected.

The Themis Slice™ architecture can handle whatever you or the outside world throw at it.

Cool.
Innovative and cost-effective cooling system can tame the hottest of processors in four 100 Watt sockets that support eight processor cores. Air and liquid heat exchanger options.

Calm.
Standardized mechanical footprint designed to survive in high shock and vibration environments - up to 40G shock and 1 grms vibration.



Collected.
Scalable - up to 16 processor cores. High-density, processor-independent architecture implemented with SPARC®, IBM®, PowerPC and x86 technology. Solaris™, Windows®, and Linux® operating systems. All networked in a single system. All managed in real-time.

Themis' Slice technology is a breakthrough in lifecycle management for mission-critical computing.

By functionally disaggregating commercial computing resources and housing them in a standardized footprint, purpose-built enclosure, Slice provides resilience with superior thermal and kinetic management. This open and modular design allows for spiral technology refresh, extending computing infrastructure investments for complete lifecycle management.

Themis' real-time resource manager integrates all computing resources, under dynamic policy control, to optimize application quality of service.

Themis Slice is transformational technology offering the most robust and efficient platform available. No other platform will enable the 21st century war fighter as effectively.

www.themis.com (510) 252-0870

THEMIS

Transformational.

Dynatem
Mission Viejo, CA.
(949) 855-3235.
[www.dynatem.com].

GE Fanuc Embedded Systems
Huntsville, AL.
(256) 880-0444.
[www.gefanuc.com/embedded].

General Micro Systems
Rancho Cucamonga, CA.
(909) 980-4863.
[www.gms4sbc.com].

Kontron America
Poway, CA.
(858) 677-0877.
[www.kontron.com].

Mercury Computer Systems
Chelmsford, MA.
(978) 256-1300.
[www.mc.com].

Motorola
Tempe, AZ.
(602) 538-5720.
[www.motorola.com/computing].

Radstone Technology
Woodcliff Lake, NJ.
(201) 391-2700.
[www.radstone.com].

SBS Technologies
Albuquerque, NM
(505) 875-0600.
[www.sbs.com].

Thales Computers
Raleigh, NC.
(919) 231-8000.
[www.thalescomputers.com].

VMEbus International Trade Association (VITA)
Fountain Hills, AZ.
(480) 837-7486.
[www.vita.com].

Serial Switched Fabrics Enable New Military System Architectures

Since no single serial switched fabric technology is ideal for the full range of military/aerospace applications, military system designers and integrators are combining multiple fabric technologies. Gigabit Ethernet is being used for the intra-platform network, with Serial RapidIO and Advanced Switching Interconnect deployed cooperatively within serial switched fabric backplanes running an identical interprocessor communications layer.

Nauman Arshad, Stewart Dewar and Ian Stalker,
Curtiss-Wright Controls Embedded Computing

The use of serial switched fabrics such as Gigabit Ethernet (GbE), Advanced Switching Interconnect (ASI) and Serial RapidIO (SRIO) in military and aerospace embedded computing systems is enabling new embedded architectures, with superior connectivity and data movement on platforms and their subsystems.

Today, using centralized or distributed GbE multilayer switches and routers, VME64x systems are evolving from parallel buses to switched architectures. Combined with IPv4/v6 protocols, GbE provides a low-cost, high-performance solution ideal for system-wide intra-platform networks (IPNs) (Figure 1). These IPNs can extend across multiple VME64x and VITA 46 backplanes to transport control data, management data and pre-processed application data. They provide a loosely coupled networking solution for seamlessly connecting platform systems—such as radar, mission computers and electronic warfare systems—into the Global Information Grid (GIG) and back into command and control using IP addresses.

Meanwhile, VITA 46 promises to revolutionize military subsystem architectures with high-speed switched serial backplanes (SSBs) that support ASI and SRIO. These interconnects, combined with a fabric-neutral interprocessor communications protocol stack, provide a tightly coupled, low-latency, deterministic framework for moving large amounts of raw data. VITA 46 is ideal for connecting multiple processors, peripherals and I/O cards within chassis. It also enables distributed switching to improve connectivity and bandwidth for demanding processing applications.

Switched GbE for IP-Based Data Traffic

Network-centric warfare is driving battlefield communications to embrace IP-based networks. Switched GbE has emerged as the preferred interconnect for high-speed, high-bandwidth IP networks within

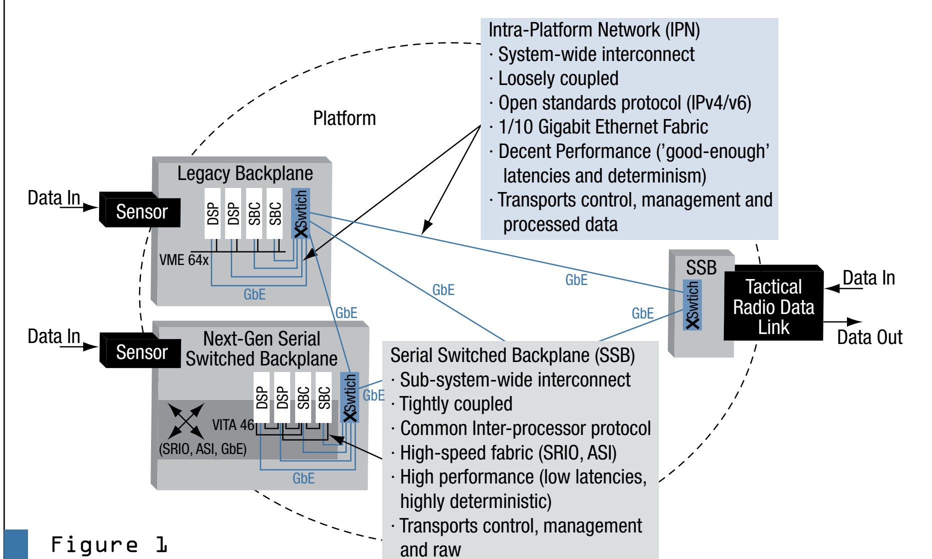


Figure 1

System-wide intra-platform networks (IPNs) and distributed high-speed switched serial backplanes (SSBs) are using Gigabit Ethernet, Serial RapidIO and Advanced Switching Interconnect.

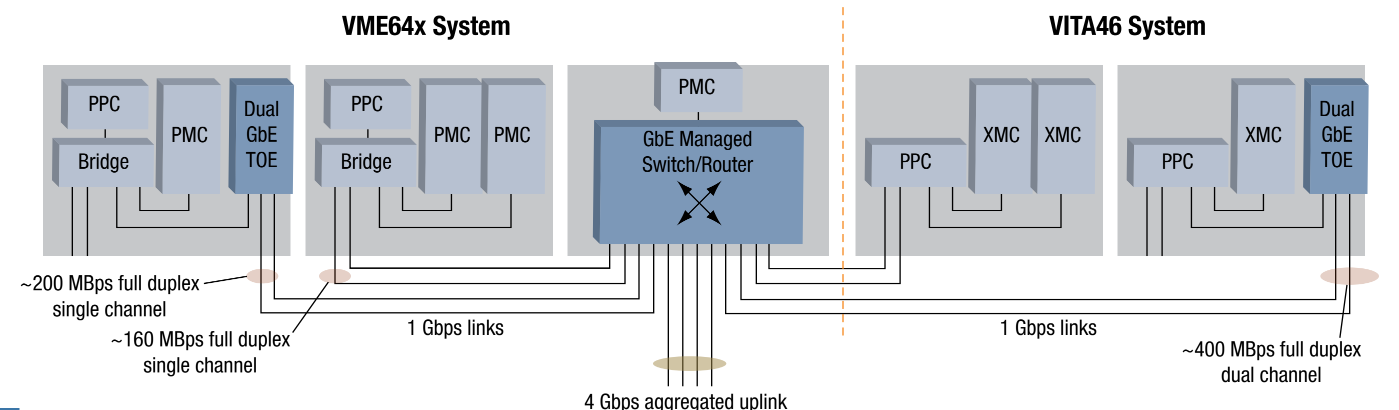


Figure 2

Beyond its use in building platform-wide networks, centralized switched Gigabit Ethernet solutions are bridging VME64x and VITA46 subsystems and extending GbE's reach into every processing node.

platforms to connect subsystems and chassis and the processing nodes within them.

Gigabit Ethernet's 1000BaseT physical layer incorporates a multilevel signal encoding method that supports simultaneous 1 Gbit/s bi-directional data transmission using only four wire pairs (8 pins) at 125 Mbaud. With minimal investment and maximized reuse of the existing VME infrastructure, system integrators can deploy a slot-based, centralized multilayer GbE switch or add distributed PMC GbE switches. The GbE-enabled VME system delivers a better connected, high-performance switched solution that communicates with IPv4 today, as well as with the DoD-mandated IPv6 in future systems.

Beyond its use in building platform-wide networks, GbE also supports the subsystem by connecting each processing node (Figure 2). Whether used to transport control, management or application data, GbE is ideal for inter-card communications in applications that do not require extremely high bandwidth and performance. Gigabit Ethernet supports star, extended star, dual star, mesh and hybrid topologies; the last three provide redundancy and failover support. Gigabit Ethernet also supports centralized and distributed switching architectures.

For high-performance, more tightly coupled GbE inter-card communication, it is possible to eliminate termination bottlenecks at end nodes, or processor cards, caused by protocol processing. One optimization strategy is to use a second CPU for protocol processing. Another approach is to use a TCP offload engine (TOE). With a TOE, throughput performance can be as high as 200 or more Mbytes/s for a single, full-duplex GbE channel and 400 or more Mbytes/s for a full-duplex channel with two GbE interfaces aggregated together. Upcoming system-on-chip solutions will incorporate multiple GbE controllers, each with its own TCP offload and DMA engines to reduce CPU loading and direct memory transfers while maximizing data throughput.

As the market shifts from Fast Ethernet networks to GbE networks, economies of scale will drive down the cost per port of GbE switch silicon, making it more cost-effective and therefore more widely used. Combined with newer high-speed serial switched fabrics like SRIO and ASI, GbE can address the most demanding application problems.

SRIO: High Throughput and Functional Density

Serial RapidIO is the single most impor-

tant element for increasing the performance of next-generation military signal processing systems. While many multi-processor algorithms rely on the flow of large data sets among compute nodes that share a problem, frequently it is performance of the transfers themselves that limit overall system performance. For decades, signal processing has demanded increasing bandwidth, which is why the VITA 46/48 module format is especially enticing for multi-processor systems. A VITA 46/48 SRIO implementation will provide 10 Gbyte/s bandwidth to the backplane, versus today's respectable 1 Gbyte/s best implementation based on VME/StarFabric.

Serial RapidIO is a point-to-point switched serial technology. Signaling rate is 1.25, 2.5 or 3.125 Gbits/s per differential TX and RX pair, or lane, yielding up to 312.5 Mbytes/s in each direction per lane. An SRIO port can have one or four lanes for a maximum data rate of 1.25 Gbytes/s per port, bi-directional. Serial RapidIO features 8-bit/10-bit encoding and end-to-end packet CRC, as well as four priority levels. It also has messaging and doorbell features for efficient inter-processor exchanges, and redundancy routes for high-availability applications.

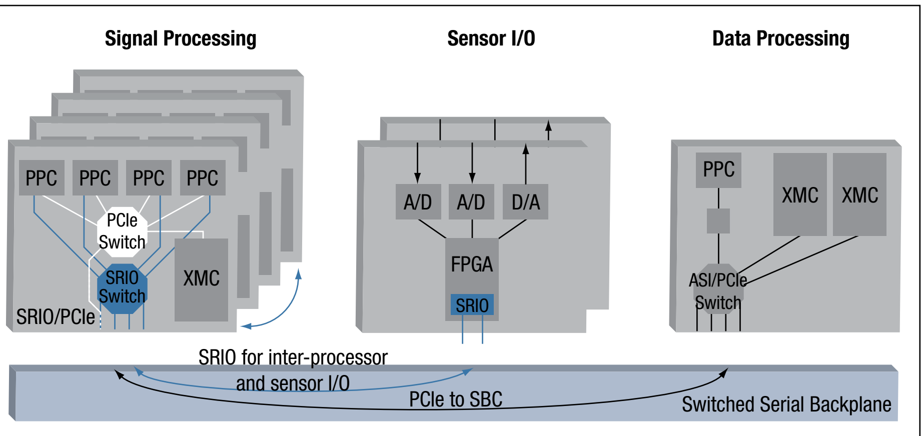


Figure 3

A generic sensor data processing system demonstrates the use of Serial RapidIO as both an on-card fabric between SRIO-equipped PowerPC devices and as a backplane fabric to data capture cards.

The VITA 46/48 standard is based on the concept of a core fabric connector intended as the board-to-board communications medium, or switched serial backplane. With SRIO, the core fabric consists of four 4-lane SRIO ports. The fastest of the current generation of fabrics, SRIO uses 3.125 Gbits/s signaling to achieve 1.25 Gbytes/s in each direction on each port, for a total bi-directional capacity of 10 Gbytes/s. With a more efficient packet structure than its peers, SRIO delivers better payload throughput under some conditions. It also permits flexible network topologies, allowing system designers to optimize implementations to suit the algorithm's data flow (Figure 3).

In addition to its superior performance,

signal processing systems can benefit from SRIO's density and power efficiency. Embedded processor providers are adding SRIO interfaces to their next-generation chips, which will reduce the number of onboard I/O devices, enabling more silicon devoted to the compute job itself. With SRIO performing data movement, multi-processor devices will also need to include both PCI Express (PCIe) and Ethernet interfaces to connect to standard mezzanine I/O modules and external TCP/IP networks.

DSP application designers will depend on high-performance, low-overhead communications software interfaces in order to achieve the goal of hardware abstraction without penalizing performance. Curtiss-Wright has implemented such software in its Inter-Processor Communication (IPC) library that currently supports PCI and StarFabric connections. Future versions of IPC will support SRIO to provide users with a software-compatible path to optimize performance in next-generation VITA 46/48 systems.

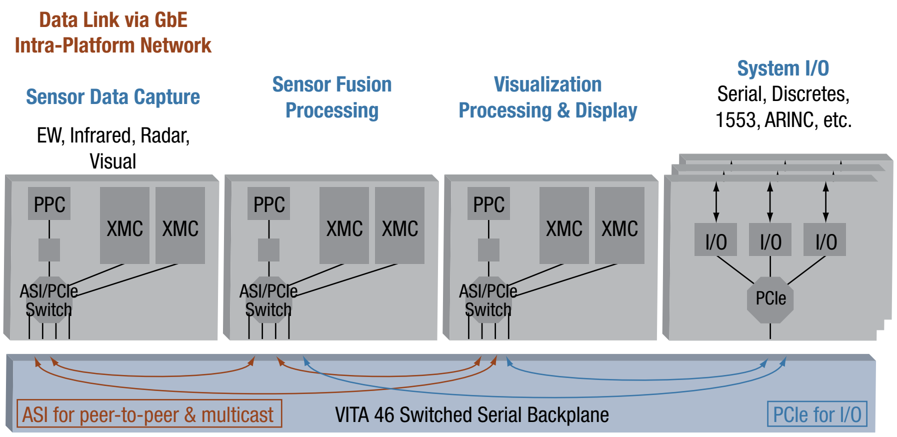


Figure 4

A conceptual aircraft mission computer illustrates the use of Advanced Switching Interconnect backplane ports in native ASI mode for processor-to-processor communication of high volumes of sensor data, and the optional PCI Express mode for communication with PCIe-based I/O cards.

PCIe Interoperability Gives ASI a One-Two Punch

Because ASI provides PCIe interoperability, it can interface to switched serial backplanes in either its native ASI mode, or as a PCIe extender for connection to I/O cards and/or PMC/XMC carrier cards. This dual-mode capability provides military/aerospace system integrators a lot of flexibility in how they employ ASI-based SBCs. Native ASI backplane ports can be used when processor-to-processor connectivity is required, and the PCIe mode when I/O expansion is required.

Because ASI has roots in PCIe at the physical and logical protocol levels it shares many of PCIe's performance, scalability and system integrity features. A 2.5 Gbits/s sig-

GE Fanuc Automation

World-Class Solutions for World-Class Challenges

When the time comes to put your trust in a technology partner for the world's most demanding military applications, put your trust in GE Fanuc Embedded Systems. With GE Fanuc as your partner, you'll be teaming with an industry leader with a long and successful history of providing the military market with world-class solutions for world-class challenges.

GE Fanuc can quickly and effectively deliver a customized application for your specific requirements. We can also provide an off the shelf portfolio of SBCs, switches, controllers, rugged flat panel monitors and PCs, networking devices and much more, to meet your wide range of embedded computing needs. When the choice means this much, choose GE Fanuc.

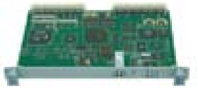
Learn more at gefanuc.com/embedded

VME-7807
Intel® Pentium M VME
Single Slot Single Board Computer

- VITA 31.1
- Processor speeds up to 1.8 GHz
- Up to 1.5 GB DDR SDRAM
- 64-bit, 66 MHz PCI-X PMC site
- Dual 10/100/1000 Ethernet
- 10/100 Ethernet
- Four 16550-compatible serial ports
- Four USB 2.0 ports
- SVGA support on the front panel
- Serial ATA interface
- Up to 1 GB CompactFlash

RM921
VME Managed Gigabit
Ethernet Switch with IPv6

- IPv6 support
- Layer 2/3/4 switching
- Twelve and twenty-four 10/100/1000 Ethernet port (front panel) options
- Copper and fiber connection options
- Full management support
- 802.1p, 802.1Q VLAN, deep packet filtering, link aggregation, Rapid Spanning Tree (802.1w, 802.1d), broadcast storm Control, port mirroring



VME-5565
Ultrahigh Speed Fiber Optic Reflective
Memory with Interrupts

- Available in PMC, PCI, and VME form factors
- Easy-to-use shared memory network-operating at 2.12 Gbaud
- Low latency for real-time applications
- Network transfer rates up to 174 Mbyte/s
- Data connections up to 10 km (single-mode fiber)
- DMA controller
- Operating system and architecture independent
- Ultra low CPU overhead, onboard hardware manages communication protocol

Sentinel
Ruggedized Flat
Panel Monitor

- 10.4, 15, 19, and 21 inch AMTFT display sizes
- Optional touchscreen, picture-in-picture video (PAL/NTSC)
- Video signal support includes: VGA, SOG, NTSC, RS170, PAL, S-video and DVI
- Compliance for shock (MIL-S-901D, Grade A), vibration (MIL-STD-167-1), EMI/EMC (MIL-STD-461E) and environmental (MIL-STD-810E)
- Anti-reflective and anit-glare coatings
- Field replaceable backlights and power supply

GE FANUC

Embedded Systems

naling rate per differential TX and RX pair, or lane, yields a nominal data rate of 250 Mbytes/s bi-directional per lane. An ASI port can have 1, 2, 4, 8, 16 or 32 lanes, for a maximum data rate of 8 Gbytes/s per port bi-directional, or for a more typical 4-lane port, 1 Gbyte/s in each direction. Advanced Switching features prioritization of data flows, or quality of service, 8-bit/10-bit encoding and end-to-end packet CRC. In addition, ASI's physical layer supports bit scrambling to reduce EMI; that is, it eliminates long sequences of ones or zeros that create a square wave.

Advanced Switching extends PCIe with several switched fabric capabilities. It supports true peer-to-peer communication models, such as load/store, queue-based and socket-like RDMA. It has flexible topologies, such as point-to-point, star, dual-star, full mesh and cascaded partial meshes, and supports multi-casting, redundant paths and failover mechanisms.

The combination of ASI's native capabilities and its PCIe interoperability makes it ideal for applications where multiple co-operating SBCs tackle sensor data processing and mission management (Figure 4). For example, modern tactical aircraft mission computer systems typically include a wide variety of functionality. This includes capturing multiple video and other sensor data streams, generating multiple graphics outputs and displaying captured video in any-to-any fashion, that is, any video input displayed on any graphics output. In addition, these systems may also include multiple SBCs for sensor-fusion processing and processing of IR video and I/O boards for system interfacing purposes, such as navigation data, weapons management, subsystem status and control discretes.

In these mission computer systems, the ASI switched serial backplane provides the required raw data throughput. It can take advantage of multicasting to reduce processor overhead and backplane loading, and it provides PCIe-compatible connections to the I/O cards so they can be managed via standard PCI software enumeration and driver software.

These new serial switched fabric technologies will drive military/aerospace embedded systems to new levels of functional density while reducing system cost and weight. Gigabit Ethernet will be used for IP-based data traffic on intra-platform networks or within a standard backplane-based subsystem and SRIO for interconnecting dense multi-computing clusters in DSP applications. ASI, with its PCIe interoperability as the flexible fabric of choice, will be used for the full spectrum of military embedded computing applications.

Because no single serial switched fabric technology is optimal for the full range of military/aerospace applications, providers of standards-based embedded computing solutions, such as Curtiss-Wright Controls Embedded Computing, deliver a broad portfolio of technologies and solutions. These include GbE for the intra-platform network, with SRIO and ASI being used cooperatively within serial switched fabric backplanes running an identical interprocessor communications layer. This approach provides system integrators with the opportunity to use the most effective switched fabric technology for each aspect of their system.

Curtiss-Wright Controls Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

Higher Throughputs Drive Advanced Signal Processing Applications

Using switched fabrics that offer multiple vendor support at the chip and board level, VITA 41 and VITA 42 support throughput of up to 10 times higher per 6U slot. This growth in bandwidth enables advanced signal processing solutions for radar, signal intelligence and image processing.

Andrew Reddig, President and CTO
TEK Microsystems

High-performance embedded computing designs have an insatiable need for bandwidth, both for ever-increasing sensor I/O requirements in and out of a system and for signal and image processing solutions within the system. Legacy switched fabrics such as RACE++, SKYchannel, Myrinet and StarFabric extended the base VMEbus standard to support high-performance signal processing applications.

The latest open standards—VITA 41 (VXS) for 6U cards and VITA 42 (XMC) for I/O modules—support throughput of up to 10 times higher per 6U slot using switched fabrics that offer multiple vendor support at the chip and board level. More advanced signal processing solutions are taking advantage of this growth in bandwidth to enable radar, signal intelligence and image processing applications that were not achievable with legacy technologies (Figure 1).

Switched Fabrics

Next-generation interconnect standards are based on the use of high-speed, point-to-point serial connections between devices. In VXS, links connect payload and switch cards in larger systems, and in smaller topologies, links are made between payload cards. In XMC, links connect an I/O module and a carrier card, which itself might be a VXS payload or switch card.

Both VXS and XMC are layered standards, defining a common mechanical interface while supporting multiple alternatives for switched fabric protocols. Many switched fabrics—such as PCI Express (PCIe), Serial RapidIO (SRIO) and Advanced Switching Interconnect (ASI)—share common electrical and signaling characteristics. This allows integrators to mix fabric-agnostic products using FPGAs with single-fabric solutions using off-the-shelf silicon.

PCI Express is defined by the PCI SIG and is used in PCs as a replacement for legacy parallel PCI and PCI-X buses. Serial RapidIO is defined by the RapidIO Trade Association and is based on the layered RapidIO switched fabric, available in both parallel and serial formats. Advanced Switching is defined by the Advanced Switching Interconnect SIG as a peer-to-peer evolution of PCIe. In each case, the VXS and XMC standards build on existing switched fabric protocols, leveraging existing standards and silicon ecosystems.

All of the fabrics share common physical interface characteristics. PCI Express and Advanced Switching are based on 8-bit/10-bit encoding with a 2.5 Gbit/s bit rate, resulting in throughput of 250 Mbytes/s for each signal pair. Serial RapidIO supports both 2.5 and 3.125 Gbits/s, allowing throughput of up to 312.5 Mbytes/s per signal pair. All of the

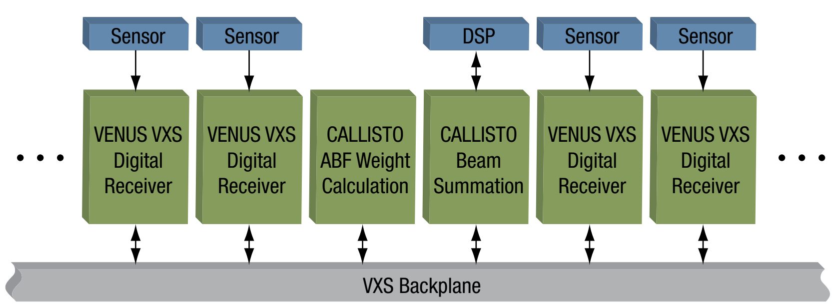
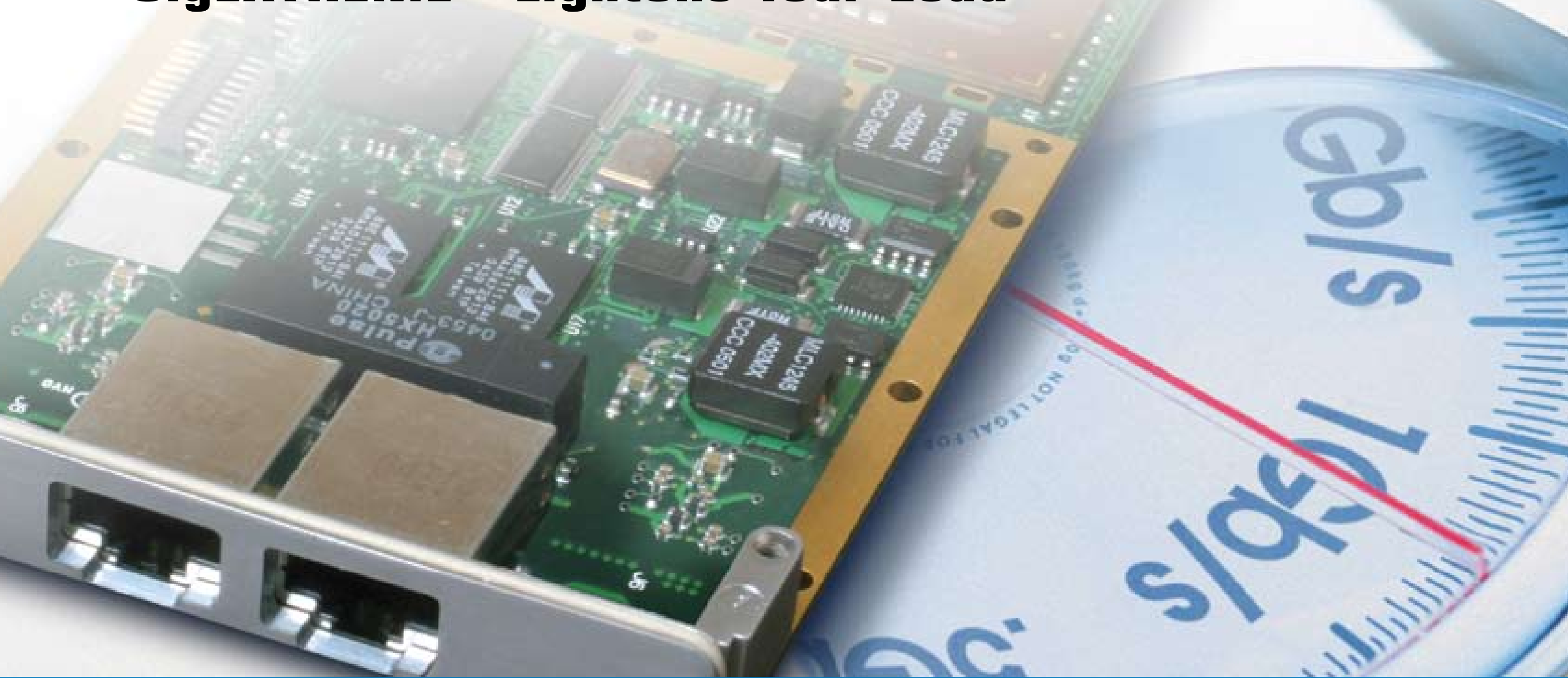


Figure 1

The increased bandwidth of VXS can increase system capability and reduce size and complexity in applications such as advanced radar adaptive beamforming. VXS cards can be combined in such a system using communication standards such as VITA 55.

Need Military Gigabit Ethernet?

GigEXTREME™ Lightens Your Load



ET-71000 GigEXTREME™ TCP/IP Offload Engine

	GigEXTREME™	Other TOE Cards	NICs with Partial Offload
Processor Loading*	**5%**	**5%**	**50% to 70%**
RTOS Support	✓	✓	—
No Application Modification or Recompilation Needed	✓	—	✓
No Use of Upscreened Commercial Components	✓	—	—
Military Rugged	✓	**Some**	**Some**
IPv6 Capable	✓	—	—

* Processor loading measured for the TCP/IP receive network task on a 1 GHz Power PC host.

Toll Free: 1-800-DDC-5757 **Web: www.ddc-web.com** **E-mail: info@ddc-web.com**

DDC®
®Data Device Corporation
ISO 9001:2000 REGISTERED

fabrics have roadmaps that take them to bit rates of 5 and 6 Gbits/s and more efficient encoding, thus offering future growth to twice the current throughput.

Supported Topologies

Although most switched fabric interconnects use a common physical layer, there are significant differences in their capabilities and, in particular, in the topologies supported.

PCI Express was designed primarily to serve as a replacement for the legacy PCI parallel bus. It uses high-speed serial interconnect technology to replace parallel buses, increase bandwidth and reduce pin count. The software model for PCIe, essentially unchanged from PCI, is based on a hierarchical tree structure. With the use of non-transparent bridging and non-

	PCI Express	Serial RapidIO	Advanced Switching
VITA 41 (VXS)	VITA 41.4 8 x 2.5 Gbits/s 2.0 Gbytes/s	VITA 41.2 8 x 3.125 Gbits/s 2.5 Gbytes/s	VITA 41.4 8 x 2.5 Gbits/s 2.0 Gbytes/s
VITA 42 (XMC)	VITA 42.3 16 x 2.5 Gbits/s 4.0 Gbytes/s	VITA 42.2 16 x 3.125 Gbits/s 5.0 Gbytes/s	VITA 42.3 16 x 2.5 Gbits/s 4.0 Gbytes/s

Table 1

Figure 2

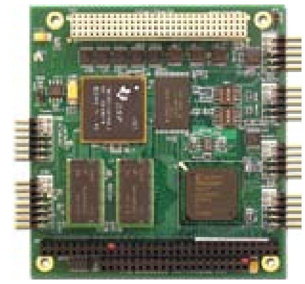
QinetiQ's Callisto VXS-1 switch card (top) and TEK Microsystems' JazzFiber PMC I/O module (bottom) provide interoperability within the VXS ecosystem of board-level components. Callisto combines a high-density FPGA processing platform with a digital I/O architecture that provides full-duplex I/O bandwidth of up to 230 Gbits/s. The JazzFiber PMC is a protocol-agnostic fiber-optic PMC I/O module optimized for both streaming I/O and signal processing applications.

RTD Embedded Technologies, Inc.

"MIL Value for COTS prices"™

Intel Celeron cpuModules™

VIA Eden cpuModules™



8000 MIPS dspModules™

cpuModules™ –40 to +85°C

		Intel Celeron™				VIA Eden™				AMD Geode™					486DX	
		CME46786HX650HR	CME47786HX650HR	CMX46786HX650HR	CMX47786HX650HR	CME36786HX1000HR	CME37786HX1000HR	CML36786HX1000HR	CML37786HX1000HR	CMG26686HX333HR	CMG27686HX333HR	CME26686HX333HR	CME27686HX333HR	CML27686HX333HR	CMV6486DX100HR	CMi6486DX100HR
Bus	AT Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus		✓		✓		✓		✓		✓		✓	✓		
	PC/104-*Plus* PCI Bus Masters		4		4		4		4		4		4	4		
	APIC (add'l PCI interrupts)	9	9	9	9											
CPU and BIOS	CPU Max Clock Rate (MHz)	650	650	650	650	1G	1G	1G	1G	333	333	333	333	333	100	100
	ACPI 2.0 Power Mgmt	✓	✓	✓	✓	✓	✓	✓	✓							
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	256	256	256	256	256	32	32
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Fail Safe Boot ROM (KB)	768	768	768	768	768	768	768	768	768	768	768	768	768	384	384
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓							
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓
	SSD Sockets, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓							
	TFT Panel TTL or LVDS			✓	✓			✓	✓	✓	✓	✓	✓			
	SVGA Interface	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
I/O	RS-232/422/485 Ports	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	USB Ports	2	2	2	2	2	2	2	2	2	2	2	2	2		
	10/100Base-T Ethernet	1	1	1	1	1	1	1	1			1	1	1		
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	aDIO™ (Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	27		
	multiPort™(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

utilityModules™ –40 to +85°C

dspModules™

- Coprocessors
- Accelerators

Specialty I/O

- Pulse width modulator
- Incremental encoder
- Opto-isolated MOSFET
- User defined FPGA

Frame Grabbers

- Single or multi-channel
- MPEG-2 compression

Video Controllers

- Analog VG A
- TTL and DVI panel support

Communication Modules

- Copper or fiber Ethernet
- USB 2.0, Firewire, CAN, serial

Wireless Telematics

- GSM, GSM-R, CDMA
- EDGE, GPRS, SMS
- GPS, Wi-Fi, Bluetooth

Motion Controllers

- DC motor controllers
- Synchro, resolver, LVDT

Power Supplies

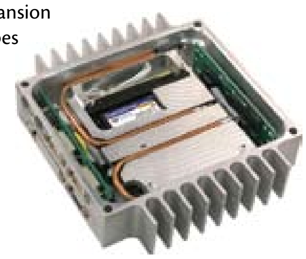
- 50/75/83/100 Watts
- Wide input range
- UPS backup
- MIL-STD-704/461

Mass Storage

- 1.8 and 2.5-inch IDE
- CompactFlash and PCMCIA

IDAN™—Intelligent Data Acquisition Node

- Build your own IDAN system
- Rugged PC/104 stacking concept
- Quick interchangeability and expansion
- Structural heat sinks and heat pipes
- Optional cooling fins
- Milled aluminum frames
- Optional MIL-SPEC paint
- Standard PC connectors
- Shock-mount isolation base



EMBEDDED-PC PC/104 MODULES

Full Product Line and Pricing Online

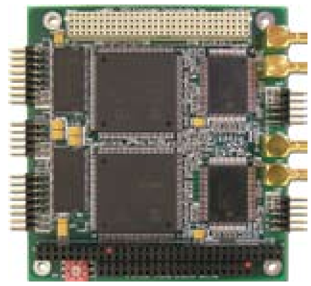
A Founder of the PC/104 Consortium • ISO9001:2001 Certified

HighRel PC/PCI-104 Modules and Systems

–40 to +85°C

Autonomous SmartCal™

Wireless Telematics



Frame Grabbers

dataModules® –40 to +85°C

		Smart A/D				Analog I/O					Digital I/O				
		SDM6440HR	SDM6540HR	SDM7540HR	SDM8540HR	DM6420HR	DM6430HR	DM7520HR	DM7530HR	DM6620HR	DM6812HR	DM6856HR	DM6888HR	DM6956HR	DM7820HR
Bus	AT Expansion Bus	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master			✓	✓			✓	✓						✓
	McBSP™ Serial Ports		✓	✓	✓			✓	✓						
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16	16						
	Differential Inputs	8	8	8	8	8	8	8	8						
	Max Throughput (kHz)	500	1250	1250	1250	500	100	1250	100						
	Max Resolution (bits)	12	12	12	12	12	16	12	16						
	Input Ranges/Gains	3/4	3/7	3/7	3/7	3/4	1/4	3/6	1/4						
	Autonomous SmartCal™	✓	✓	✓	✓										
	Data Marker Inputs	3	3	3	3	3		3							
Conversions	Channel-Gain Table	8k	8k	8k	8k	8k	8k	8k	8k						
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓	✓						
	A/D FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						
	Sample Counter	✓	✓	✓	✓	✓	✓	✓	✓						
	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓	✓	✓					✓
	SyncBus		✓	✓	✓			✓	✓						
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	16	16	48	32	64	32	48
	Bit Programmable I/O	8	8	8	8	8	8	8	8	8	24				48
	Advanced Interrupts	2	2	2	2	2	2	2	2	2	2				2
	Input FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						2M
	Opto-Isolated Inputs											16	48	16	
	Opto-Isolated Outputs											16	16		
	User Timer/Counters	2	3	3	3	2	2	3	2	3	3				10
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓
	Relay Outputs													16	
Analog Out	Analog Outputs	2	2	2	2	2	2	2	2	4					
	Max Throughput (kHz)	200	200	200	200	200	100	200	100	200					
	Resolution (bits)	12	12	12	12	12	16	12	16	12					
	Output Ranges	3	4	4	4	3	1	4	1	4					
	D/A FIFO Buffer		8k	8k	8k			8k		8k					

RTD FieldPads™

- Ruggedized, embedded computer systems
- User-specified CPU and PC/PCI-104 expansion
- Weathertight components
- Integrated 6.5-inch video panel, keyboard
- Heat pipes for high performance CPUs
- User-defined MIL connectors
- Internal and external battery packs
- Expand with any RTD PC/PCI-104 product

Industrial FieldPad™

Ideal for control and monitoring of processes on factory floors or industrial installations. Mounting flanges allow the unit to be installed on machinery or walls, enabling standard PC access in a rugged enclosure resistant to industrial environments.

Tactical FieldPad™

Designed for mobile and portable applications where the angled panel and ergonomic design allow for optimal viewing with flexible positioning. Data collection/downloading and information access accomplished through wired or wireless connections.

HiDAN™ and HiDAN*plus*™—HighRel Intelligent Data Acquisition Node

- HiDAN is a rugged, watertight enclosure for a stack of PC/104 modules
- HiDAN*plus* combines the modularity of IDAN with the environmental ruggedness of HiDAN
- Integrated tongue and groove O-ring for environmental sealing and EMI suppression
- Structural heat sinks and heat pipes
- Optional cooling fins
- Milled aluminum frames
- **Stackable signal raceway**
- Optional MIL-SPEC paint
- MIL I/O connectors
- Shock-mount optional

www.rtd.com
Specifications, manuals, drivers, and plant tour

RTD Embedded Technologies, Inc.
103 Innovation Blvd • State College, PA 16803
T: 814-234-8087 • F: 814-234-5218

"Accessing the Analog World"®

blocking crossbar switches, PCIe can be used to construct high-bandwidth systems, but it is better suited to local clusters of onboard devices.

Serial RapidIO and ASI were both initially designed as peer-to-peer fabrics. Both include standardization of autodiscovery, fault tolerance, load/store and messaging semantics, flow control and multicast. In addition, both support a wide range of topologies beyond simple tree hierarchies. In a VXS- or XMC-based system, SRIO and ASI are well suited to provide a chassis-wide or even multi-chassis switched fabric interconnecting all nodes in a system. The choice of which switched fabric to use depends on the available ecosystem for each option.

Board-Level and Chip-Level Ecosystems

From a system integrator's perspective, the ecosystem consists of board-level components such as XMC I/O modules, XMC carrier cards, VXS payload cards and VXS switch cards. To build systems based on open standards, the integrator must be able to source components that provide the required performance along with interoperability with other vendors' products (Figure 2).

In turn, board-level products are enabled by the underlying chip-level ecosystem. Although FPGAs can be used to provide highly flexible solutions for many applications, especially as fabric-agnostic endpoints, the use of FPGA technology for core elements of the solution often results in higher power and cost. In systems that require full switched fabric connectivity, merchant silicon is typically needed to provide acceptable cost/power tradeoffs.

The chip-level ecosystem consists of several different elements. The core chip-level component of a switched fabric ecosystem is the switch itself, providing the interconnect between other switches and endpoints. In some applications, an FPGA-based switch can be used to provide static routing of point-to-point links. However, an ASIC-based switch is usually needed for full switched fabric connectivity.

Switch silicon is currently available for PCIe in densities ranging from 4 ports/16 lanes to 8 ports/32 lanes, or up to 64 Gbits/s aggregate bandwidth. Serial RapidIO switches are available in 4- and 8-port versions with 80 Gbits/s of aggregate bandwidth. Advanced Switching switches are becoming available both with and without integrated PI-8 bridges to directly support up to 10 ports of PCIe or ASI connectivity and 80 Gbits/s of aggregate bandwidth.

One advantage of ASI switches is the availability of integrated PCIe, or PI-8, bridges within the switch. Because ASI is designed as an evolution of PCIe technology, most ASI switch vendors are designing switches with integrated bridges to leverage existing PCIe endpoints. This provides a highly integrated solution for mixing PCIe and ASI devices in a system.

Another key component consists of bridges from legacy bus interfaces such as PCI and PCI-X into newer switched fabrics. In this area, PCIe's close connection to the older ecosystem provides an advan-

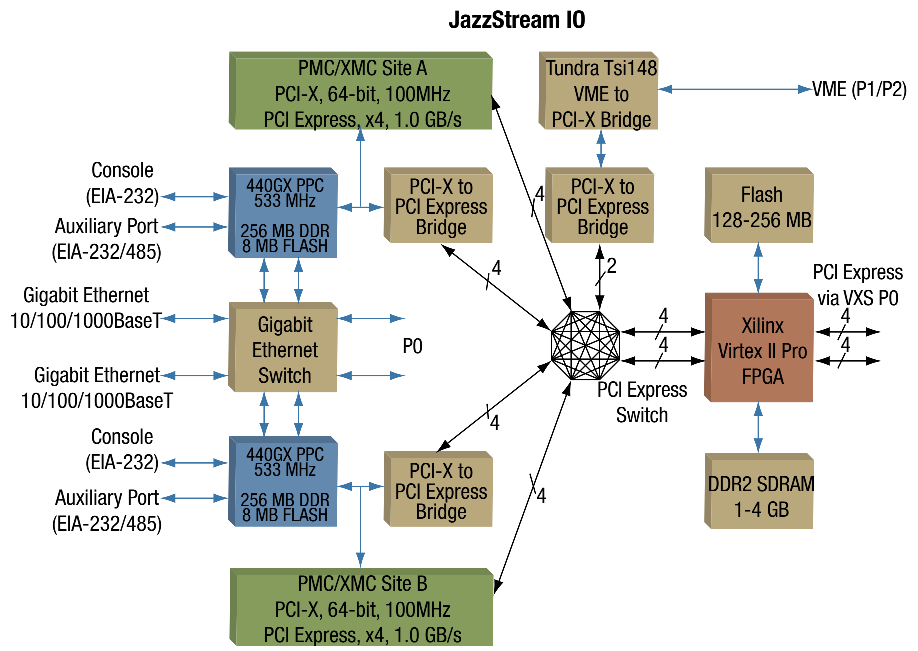


Figure 3

The JazzStream IO carrier card can support VITA 55 interconnect for point-to-point connections, or bridge to larger PCI Express, Serial RapidIO or Advanced Switching Interconnect system-wide fabrics.

tage, with bridge solutions available from multiple vendors. Older I/O solutions based on PCI and PCI-X can be upgraded to support PCIe through the use of relatively inexpensive and low-power ASIC bridges. The same bridge solutions can be used to interface with an ASI fabric when using switches with integrated PI-8 bridges. While PCI and PCI-X can be bridged to SRIO through FPGA-based interfaces, there are no SRIO/PCI bridge chips available today.

Bridges from legacy bus interfaces to switched fabrics are necessary during the transition period when legacy bus interfaces are integrated with newer switched fabric technology. Ultimately, however, the devices that use legacy interfaces will be upgraded to act directly as switched fabric endpoints, supporting higher bandwidths while dramatically reducing pin count and package size.

Most of the activity in this area has been in the PCIe arena, driven by the larger PC-compatible marketplace. Merchant silicon solutions are shipping today for a wide range of I/O interfaces, including single- and multiple-channel Gigabit Ethernet (GbE), Fibre Channel and Serial ATA, along with high-speed graphics interfaces. Again, the use of integrated PI-8 bridges allows ASI switches to interface directly to PCIe endpoint devices.

Many types of sensor I/O interfaces are being implemented using FPGA technology. Interfaces such as Serial FPDP, and tailored GbE and Fibre Channel solutions, can be implemented with an FPGA to provide both the sensor interface and additional front-end signal processing. These types of interfaces are usually fabric-agnostic and use FPGA-based IP cores to interface to the required fabric. FPGA interface solutions are available for PCIe, SRIO and ASI.

Finally, the last component, and the one with the longest development cycle, is the processor itself. In high-performance embedded computing, general-purpose processing is still focused on PowerPC technology. The latest PPC processors from AMCC and Freescale have embedded fabric interfaces and support integrated PCIe interfaces. The Freescale portfolio also includes processors with interfaces selectable between SRIO and PCIe. Serial RapidIO has an advantage over ASI with its processor options that directly support SRIO without additional bridging.

Alternatives to Switched Fabrics

Although switched fabrics provide maximum flexibility for larger systems, a number of applications can benefit from a simpler approach. Smaller systems, including radar and SIGINT solutions, can often be built without a fully switched fabric interconnect because the data paths are well defined at the outset. These systems may still use VXS and XMC building blocks, but can utilize point-to-point links without switched fabric dynamic routing.

To support interoperability between cards in smaller systems using non-fabric links, TEK Microsystems, QinetiQ and Mercury Computer Systems have co-sponsored the new VITA 55 standard. VITA 55 defines a lightweight protocol for point-to-point interfaces between cards in a system without the overhead or complexity of switched fabric endpoints or routing. FPGA-based endpoints can easily support VITA 55 along with more complete PCIe, SRIO and ASI solutions through the use of FPGA IP cores.

Implementation

One example of a solution that combines PCIe technology with VITA 55, SRIO and/or ASI is TEK Microsystems' JazzStream IO carrier card (Figure 3). The JazzStream card uses an onboard PCIe switch to interconnect two PowerPC control processors and two PMC/XMC I/O modules. An FPGA-based bridge is used to connect the PCIe switch to the backplane through a VXS connector. The use of an FPGA bridge allows the card to support VITA 55 interconnect for point-to-point connections or a bridge into larger PCIe, SRIO or ASI system-wide fabrics. The system software manages the details of the FPGA bridge, allowing the user application to use a common set of API calls to participate in any supported system-wide fabric. ▮▮

TEK Microsystems
Chelmsford MA.
(978) 244-9200.
[www.tekmicro.com].

Key Design Techniques Reduce EMI/RFI Effects in Military Applications

EMI/RFI effects increase in high-speed, high-performance military designs. Careful preparation, planning and interaction between OEM and EMS provider, along with the correct implementation of five key design measures, can reduce EMI/RFI by 90% or more.

Zulki Khan, President and Founder
Nexlogic Technologies

The effects of electromagnetic interference (EMI) and radio frequency interference (RFI) are particularly troublesome when designing printed circuit board (PCB) assemblies for high-speed military and aerospace systems. The components on a PCB may be digital and analog. Transmission lines connecting the two different sections are used to transmit signals back and forth. Unfortunately, as frequency increases and signals are enhanced, noise related to those frequencies is also enhanced, thus creating EMI and RFI.

Electronic systems are expected to operate normally within a given environment without internally or externally radiating excessive amounts of electromagnetic energy. In this state, they are called electromagnetically compatible (EMC).

However, when electromagnetic energy is radiated adversely it becomes EMI, disrupts circuit performance and makes overall PCB operation less optimal, falling short of original design goals. The two main sources of electromagnetic radiation from a PCB are radiation from signal loops and circuit tracks.

The radio frequencies that are by-products of an electronic device's operations range from about 10 kHz to 100 GHz. These can be either radiated emissions through a medium such as an electromagnetic field, or conducted emissions through a medium such as a propagating wave through wire or interconnect cables.

Successfully reducing EMI/RFI calls for careful preparation, planning and close interaction between an OEM and an electronic manufacturing service (EMS) provider. Further, the EMS provider must focus on a set of five key design measures to significantly suppress EMI/RFI effects. These are using differential pairs, multilayer PCB construction, shielding clock signals, properly placing analog and digital components and properly bifurcating power and ground planes (Table 1).

By carefully and correctly implementing these design steps, EMI/RFI can be reduced by 90% or more. Omitting or giving little attention to any one of them can boost EMI/RFI to increase noise and crosstalk levels well beyond a design's specifications, thus impeding proper signal transmission and reception.

Differential Pairs

Differential pairs refer to the traces that provide paths for transmitting and returning current (Figure 1). These parallel traces are separated by a minimum distance. Tolerance is normally to within 10% in order to reduce EMI. For example, if a transmit line is 10 mils long, then the return path should be 9 to 11 mils long. Hence, the difference between the two should be 10% or less. In military and aerospace applications, differential pair tolerances in extremely high-frequency, high-speed circuitry must be considerably less than this at 5%.

If tolerances exceed these low percentages and increase to 20% or 25%, for instance, the transmit path becomes shorter than the return path by 20% to 30%. Hence, transmit-to-receive ratios become unbalanced, causing increased EMI/RFI. PCB layout software packages, such as Cadence Allegro or Mentor Graphics' PADS Power PCB, can alert designers to differential pair tolerance variances.

PCB Layer Construction and Geometries

For high-density, high-speed applications, multilayer PCBs containing multiple power and ground planes are used. Compared to single- or double-sided boards, these PCBs greatly reduce the effects of EMI/RFI and allow designers to closely control impedances on certain layers. They also allow high component densities and make it easier to route signal and power tracks.

Layer construction can play a vital role in reducing EMI/RFI. Symmetrical stripline geometry is the best approach in minimizing or eliminating EMI/RFI. A single signal layer is sandwiched between two ground layers so the ground planes absorb virtually all noise and crosstalk. In addition, ground plane redundancy suppresses all noise and crosstalk.

One electrical requirement of an efficient circuit is providing a low impedance path for current to return to its source at both DC and high frequencies. Therefore, it must have low resistance and inductance. Symmetrical stripline geometry delivers an ideal balance for EMC because its solid ground plane provides a stable reference for all the board's current returns.

Coplanar geometry is RFI-specific, and also helpful for reducing EMI. It creates an antenna effect, or solid closed loop, to provide a clear signal path. As much solid ground is made possible on both sides of a trace so that a signal passing through that trace is heavily guarded.

Shielding Clock Signals

Clock circuits generate digital circuit pulses at regular intervals, which are critical to circuit performance. Clock circuitry is especially sensitive to noise and crosstalk because clock signals must be clean for the circuitry to perform its function. The high clock speeds needed in many military/aerospace designs require properly managing board-level design, layout and signal

Five Key Design Measures for Suppressing EMI/RFI

Key Design Measure	Design Objective
1. Differential Pairs	1. Five to 10% tolerance between transmit and return traces.
2. Layer Construction	2. Signal layer sandwiched between two ground layers to absorb noisy crosstalk.
3. Shielding Clock Signals	3. Shielding clock circuitry, adequate spacing between different traces, and ground shielding to protect clock or digital signals running through analog circuitry.
4. Proper Component Placement	4. (a) Isolate noise-generating components from less noisy ones that are highly sensitive to EMI/RFI. (b) Separate analog and digital components so that traces can be easily, but separately, routed underneath the proper return path, ground, and power planes.
5. Bifurcate Power and Ground Planes	5. Power and ground planes under the trace layers are bifurcated in between the power and ground sections. As a result, signals under the analog and digital sections are clean and well-segregated to reduce EMI and suppress noise.

Table 1

EMS providers must focus on a set of five key design measures in order to significantly suppress EMI/RFI effects on a PCB design. When these design steps are implemented carefully and correctly, EMI/RFI can be reduced by 90% or more.

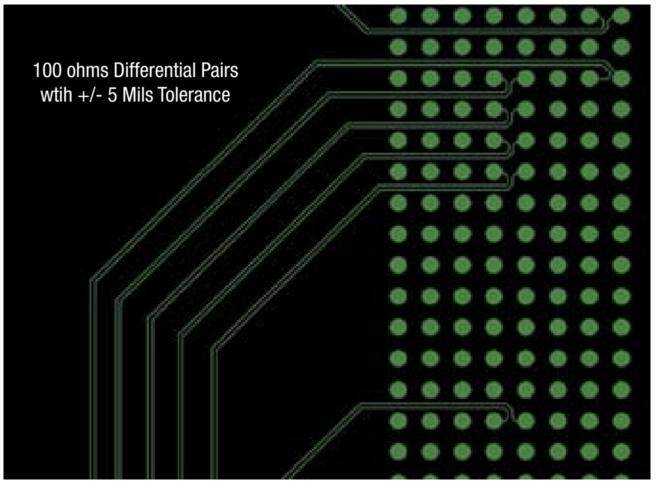


Figure 1

100 ohm differential pairs are traces that provide paths for transmitting and returning current, separated by a minimum distance. In this layout, the traces shown running next to each other are maintaining 5% tolerance for the length matching.

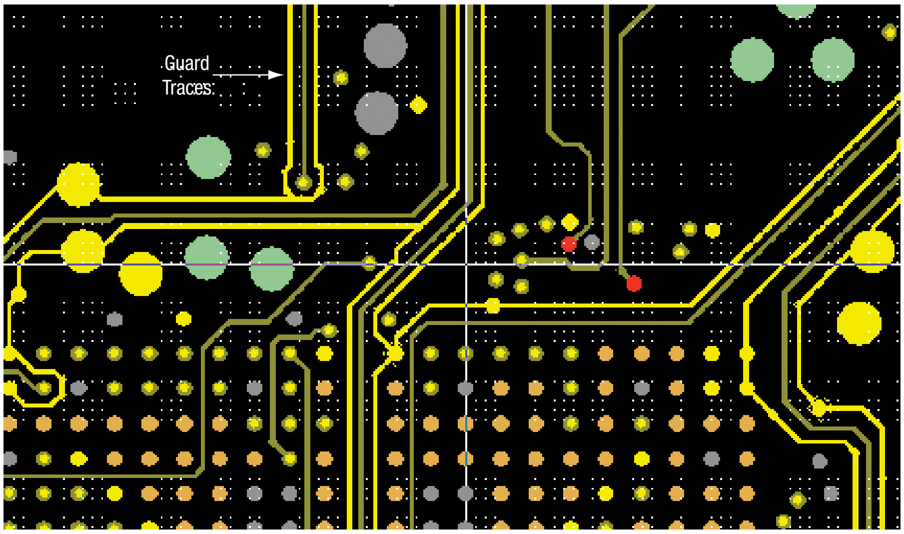


Figure 2

The clock traces of a digital circuit are shown with GND-shielded guard traces so that the signal flow is clean and protected from noise.

Clock circuitry is the most critical section in a mixed-signal PCB.

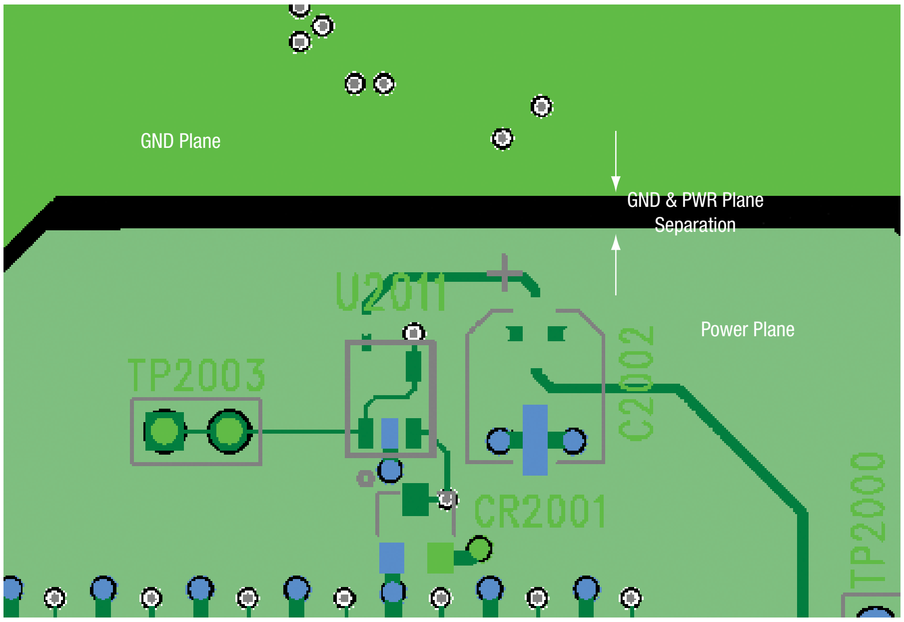


Figure 3

Signals transmitted underneath analog and digital components must be clean and well segregated. An internal layer of a multilayer PCB is shown with power and ground layers split for proper signal transmission.

interconnects. High-speed switching can produce electromagnetic waves that generate resonance, power/ground bounce, simultaneous switching noise, reflections and coupling between traces and power/ground planes.

Properly shielding clock circuitry is critical as a major step in reducing EMI/RFI (Figure 2). This is achieved by maintaining an adequate amount of spacing between traces once clock circuitry has been routed. The "three width (3W) rule" is applicable here. For example, if a clock signal is 5 mils wide, then it should be separated from corresponding traces and signals by 15 mils.

Clock circuitry is the most critical section in a mixed-signal PCB. When these signals must run through noisy analog circuitry because those paths cannot be avoided, ground shielding must be performed to protect clock signal traces or critical digital signals. It is best to run a clock net and use a ground trace to shield the clock trace's entire path.

Proper Component Placement

Two component placement techniques are normally used to reduce EMI/RFI effects. One technique ensures that the noise-generating components are isolated from those components that generate less noise and are highly sensitive to EMI/RFI. For example, a high-speed crystal with high signal spikes must be isolated from sensitive clock signals. These components operate at different frequencies, creating different waveforms. Hence, the closer together they are, the more noise and crosstalk will be generated and amplified. Noise-generating components should thus be separated at a specified distance from others on the PCB.

Correct component placement is also vital for mixed-signal and digital PCB design. High-power, high-current analog circuits inherently create noise, which can adversely affect adjoining low-power, low-current digital circuits if proper partitioning between the two is not correctly implemented.

An example of effective partitioning places power supplies, analog interface converters and other analog circuits on

the left side of the board, while high- and low-frequency digital components are placed on the right side; the system clock is in the middle and connectors are located at the board's edge. In this way, analog and digital components are totally separated and traces can easily be routed separately.

Signals transmitted underneath analog and digital components must also be clean and well segregated. An internal plane layer underneath the trace layers may be bifurcated so that power and ground layers are split for proper signal transmission (Figure 3). This technique reduces EMI effects and suppresses noise.

Ideally, the analog section must be totally isolated in terms of placement, routing and plane separation. Analog traces should run only underneath their analog reference power or ground plane. Conversely, digital traces should run under the digital section with respective power and ground planes. Impedance is thus kept constant, and there is a good return signal path.

Using Radius Bends and Blind/Buried Vias

When routing RF circuits, it is important to avoid the extreme bends at 45° angles that many digital designers rely on to conserve routing space. These angles hinder proper propagation to high-frequency performance, causing impedance mismatches. Using arcs instead of sharp angles eliminates this problem.

A high-frequency effect created by this conventional PCB layout practice is return loss reflection, which cancels an incoming signal due to out-of-phase reflections. This problem can be resolved by using mitered corners or a radius bend to change the trace's direction.

Blind vias, as the name implies, go from an external layer—such as the component or solder side of the board—to one of the internal planes, whereas buried vias go from one internal layer to another internal layer.

Blind and buried vias rather than through-hole vias are more effective for minimizing EMI/RFI and maintaining high signal integrity, especially in high-speed boards. For instance, in the through-hole approach, a signal may go from the top layer to layer three, but if the hole goes all the way to a bottom layer, such as layer 12, then a stub is created. This stub is the portion of the through-hole via not used for signal transmission. In effect, the stub serves as an antenna that creates added noise. Blind vias are used to transmit signals between layers and provide exact termination at the exact layer. For example, a blind via can go from layer one to layer three and terminate at layer three, even if that PCB has 12 or more layers. ▮

Nexlogic Technologies
San Jose, CA.
(408) 436-8150.
[www.nexlogic.com].

Designing EMI/EMC Compliance into Military Systems

Ensuring that military embedded computing equipment is EMI/EMC-compliant is more than just a matter of making it conform to MIL-ST-461. Numerous design and manufacturing issues must be taken into account, as well as cost constraints and reducing the impact on size and weight.

Alan Storrow, Engineering Manager, Systems Business Unit
Radstone Embedded Computing

Electromagnetic interference compliance, or lack of it, can literally be a life or death matter when it comes to military embedded computing equipment. Ensuring that a military Air Transport Rack (ATR) chassis is fully compliant with electromagnetic compatibility (EMC) requires taking into account numerous design and manufacturing issues. In addition, cost constraints must be considered, as well as maintaining a minimal impact on factors such as size and weight, which are increasingly key concerns in military applications. In the real world outside of the laboratory or the test bench, access and maintainability, not to mention the repeatability of a solution, can also provide specific challenges to the designer.

Electromagnetic interference (EMI) can be defined as electromagnetic emissions from a device or system that interfere with the normal operation of another device or system. Electromagnetic compatibility can be defined as the ability of a device or system to function without error in its intended electromagnetic environment.

When it comes to weapons systems and defense electronics, the effects of non-compliance with EMC, i.e., the presence of EMI, can be potentially disastrous. Mindful of the potential impact of mobile phones and laptop computers on aircraft controls and medical electronics, commercial airlines and hospitals can simply ban their use rather than design for immunity.

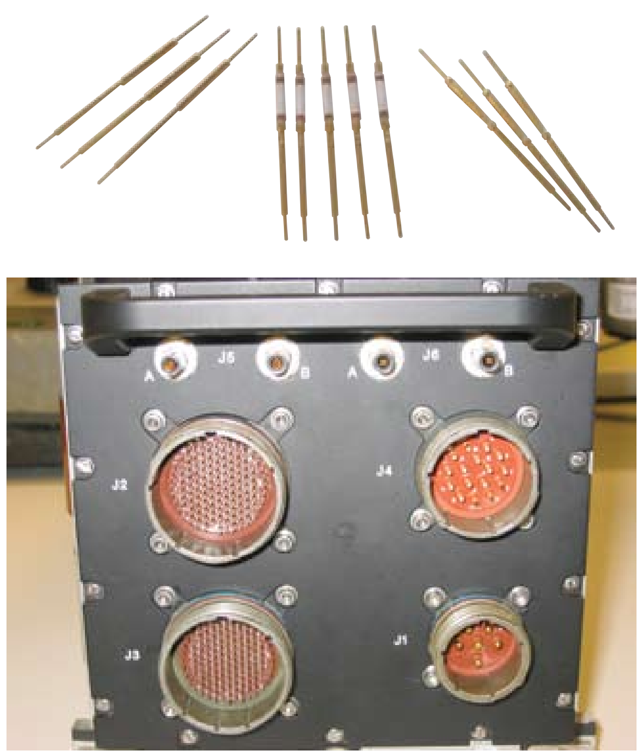


Figure 1

A 3/4 Air Transport Rack (ATR) chassis configuration (bottom) is made EMC-compliant by using grounding, feed-through and filtered contacts (top).

MISSION POSSIBLE.

At Curtiss-Wright Controls Embedded Computing, we know that reliability and longevity are a critical part of your embedded system. That's why we design, integrate and test every product we make to ensure that they'll perform in all kinds of environments, even those where service and support are nearly impossible.

That's why you should rely on Curtiss-Wright to minimize risk and maximize performance in your mission-critical embedded components and systems.

And that's The Power Within.

Dy 4 Systems | Peritek | Primagraphics | Synergy | Systran | VISTA Controls

CURTISS WRIGHT Controls
Embedded Computing

www.cwcembedded.com

Figure 2

Since they are maintenance-free, gasketless interfaces (left) are often preferred on removable panels, such as this ATR chassis lid. Gaskets are used when the chassis must prevent moisture ingress, such as this compressible o-ring gasket (right).

This is not a luxury afforded to the military, and much time and money is spent on EMC compliance testing long before equipment ever enters service. Testing is initially carried out at the subsystem level and repeated at higher tiers of integration. Problems found at the subsystem level may be relatively simple to fix, but as system integration builds so does the problems' potential complexity and the cost of their rectification. Sound EMC practices should therefore be employed from the first in the design of any new equipment and system interconnection.

Designing-in Compliance

Power leads, often unscreened in system installations, are inherently noisy and require filtering where they enter the equipment enclosure to remove higher frequency components that could interfere with operation. This may be achieved with a filtered input connector or filtered "dirty box" that encloses the input power connector, effectively trapping electrical "dirt" and ensuring that the remainder of the unit is clean. This also prevents high-frequency emissions within the enclosure from coupling onto the power rails and passing out of the equipment.

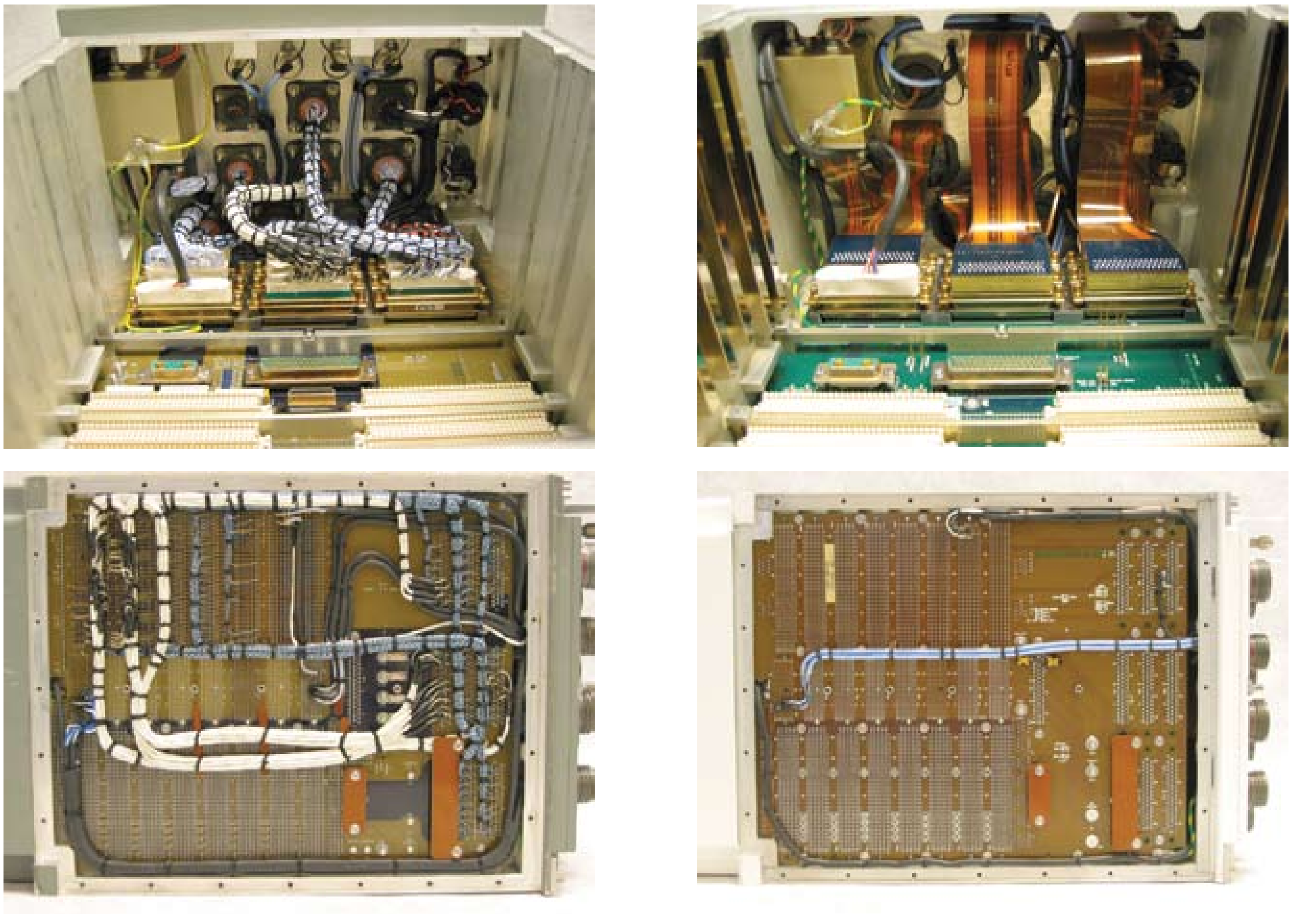


Figure 3

To address the need for consistent manufacturability, the original prototype design (left) is migrated to a production version that can be readily repeated (right). At top, the cable used in the development of the prototype (left) is replaced by flexible circuit interconnects in the production version (right). At bottom, the white cable harness used for proof of concept (left) is embedded in the backplane tracking (right).

Signal cable connections between different equipment are normally screened with an overbraid to prevent switching spikes from coupling into the signal paths. To preserve the integrity of the shield, interference currents must be diverted to the outside surface of the shield where they are confined by a "skin effect." This is an electromagnetic property that tends to confine AC current flow to the surface of a conductor.

Within this outer screen, signals run as single conductors, twisted pairs, screened twisted pair, coaxial, twinaxial, optical fiber and the like. The effectiveness of this overall screen, and of the individual conductor screens that pass through the enclosure connector, relies on a low bonding impedance between connectors and the front panel. This requires that the rear of the front panel, the connector contact face, be machined to a tight flatness tolerance for good metal-to-metal contact with the connectors. Alternatively, a metal-loaded gasket may be used that comprises not only the primary gasket material but also a metallic content which, when compressed, provides electrical conductivity.

Upgrade/Retrofit vs. New Design

In some cases, the equipment may be an upgrade to an older installation, a frequent military requirement, where screened interconnects were not used. One example of this is an avionics computer program for a multi-role aircraft in which an upgrade was necessary. One of the upgrade's requirements was that the existing cable infrastructure must remain in place. Analysis of the cabling revealed that, since it was largely unscreened, EMI problems were likely to be encountered in the new environment. The solution was to introduce filtered connectors, allowing the cabling to remain in place while bringing the overall system within acceptable EMI limits.

In other cases, the additional weight of the screen overbraids may be an unacceptable system penalty. In these situations, filters may be introduced into individual signal lines at the chassis enclosure. Connectors are available that provide for ground, feedthrough or filtered contacts that may be independently loaded (Figure 1). The individual contact element is then selected depending on signal switching speed or noise threat. Within the equipment enclosure, individual groups of signals will maintain their screens and the internal cable routing will again be a mixture of single conductors, twisted pairs, screened twisted pair, coaxial, twinaxial and optical fiber.

Connection and Gasket Solutions

Selecting and implementing appropriate connection solutions is of paramount importance in ensuring EMI compliance. In the case of an avionics defensive systems manager program, the connector choice specified by the customer was at variance with the EMI specification provided. Testing confirmed that this disparity produced a high level of radiated emissions. The customer had specified a coaxial connection, which uses its outer shield as the return path. Substitution of triaxial cable and connectors provided the necessary screening.

The enclosure itself should provide a continuous conductive screen. Aluminum is normally the material of choice, since it is a compromise that balances weight, cost, manufacturability and high thermal and electrical conductivity. The main chassis should be constructed to provide good conductivity between the various panels, as if it had been machined from a solid block of metal. The best results are achieved by brazing or bonding the individual panels together. Protective surface finishes such as alochrom or electroless nickel plate should be employed to prevent oxidization and maintain electrical integrity over many years of service. These protective finishes must be able to withstand the environmental conditions in which the system is planned to operate, including factors such as shock, vibration, humidity and corrosive atmospheres.

On removable panels, tongue-and-groove gasketless interfaces are preferred, since they are maintenance free. In some cases, such as tracked vehicles, there may be an equipment hose-down requirement, or in others, an environmental requirement such as driving rain. In such cases where the chassis is required to prevent moisture ingress, conductive, usually metal-loaded, gaskets are used (Figure 2). Consideration should also be given to the separation distance between fasteners to ensure that metal-to-metal contact is maintained along the length of the joint.

Within the system electronics, circuit card assemblies may have protection against overvoltage spikes on input/output lines and may employ techniques to filter the noise they generate, which may be conducted or radiated within the system. However, it is normally the power supply that contains the majority of noise control circuitry. As well as being required to tolerate considerable variation in the voltage from the system power generator, the power sup-

ply is also required to filter high voltage spikes and surges and to prevent them from propagating onto the internal DC supply rails. Because of stringent regulations concerning conducted emissions in both commercial and military equipment, the power supply must contain large filter elements to prevent switching spikes from being conducted back down the power lines.

EMC and Manufacturability

Consideration should also be given to the positioning and partitioning of components and cables. This includes segregating high-frequency from low-frequency power and signal wiring, system grounding and bonding, keeping screen terminations short, surge suppression and filtering, and, most importantly, build repeatability from one unit to the next. While a printed circuit board (PCB) fixes the position of the components mounted on it, a cable harness requires a disciplined approach to documentation and inspection to ensure that the design is repeated as intended, and that any test results are representative of all units built to the same build standard.

It is now common practice to supplement engineering drawings with a library of digital photographs for illustrating detail and manufacturing technique. The best method of ensuring the repeatability of interconnection routing is to integrate the I/O tracking into the backplane and use PCBs with flexible circuit interconnects to carry the signal traces to the front panel connectors. For example, cable used in the development of a system's prototype can be replaced by flexible circuit interconnects in the production version and the cable harness used for the prototype can be embedded in the production version's backplane tracking (Figure 3). The conductor types used in the wired prototype—such as controlled impedance, twisted pair, screened twisted pair, co-axial and twin-axial—are repeated in the backplane tracking and flexible circuit interconnects using standard PCB design tools.

Compliance testing applies standardized tests and methodologies, but there will always be operational modes and combinations of modes that cannot be simulated in a test house. For example, electromechanical action such as turret motion and weapon firing produce high current surges that can cause surge, spike and brownout effects on the system generators. Because not all deployed environments can be replicated, designing for EMI/EMC compliance requires the application of sound principles from the very outset and the implementation of a rigorous, disciplined and methodical approach. If these principles are applied at every tier of the development process, the risk of lack of compliance in the total system can unquestionably be minimized. ▮

Radstone Embedded Computing
Towcester, UK.
+44 (0) 1327 359444.
[www.radstone.com].

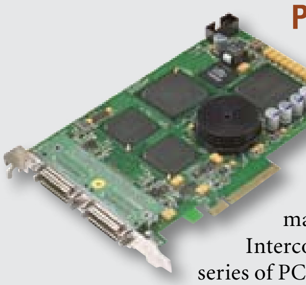
Module Adds CameraLink Connectivity to FPGA-Based PMC Board

When designing systems used for target tracking, feature recognition or real-time filtering, the ability to merge data acquisition with a local, user-programmable FPGA gives a wider range of performance options. To help facilitate this, Vmetro has introduced the CAML-MOD3 CameraLink adapter module for its high-performance Xilinx Virtex II Pro-based PMC-FPGA03 PMC module.

The CAML-MOD3 uses the rapidly emerging Mini CameraLink (MiniCL) HDR26 connector standard. It employs the MDR26 connector for traditional CameraLink equipment. In Base mode, up to two cameras can be attached to the CAML-MOD3/PMC-FPGA03 combination via separate cables. In Medium and Full modes, a single camera can be connected via two cables. The CAML-MOD3 supports the maximum CameraLink clock rate of 85 MHz, allowing real-time sustained data rates of up to 680 Mbytes/s into the FPGA in Full mode. An efficient 64-bit PCI interface supplies the bandwidth necessary to transfer processed or raw video to the PMC host carrier.

Developers can implement their own proprietary processing algorithms for capturing CameraLink data with the provided example firmware (VHDL) and host software (C++). Comprehensive PMC-FPGA03 library firmware for communicating with PMC-FPGA03 board resources, and host library software for implementing register and DMA-based board communication, further simplify the development process. Single-unit pricing is $995.

Vmetro, Houston, TX. (281) 584-0728. [www.vmetro.com].



PCI Express Adapter Cards Deliver Low Latency

Multi-processing, multi-node real-time applications, such as mobile defense electronics on the battlefield, need to move large volumes of data at high bandwidth between many systems. With this in mind, Dolphin Interconnect Solutions has released the D350 series of PCI Express adapter cards that combines high data throughput with low latency.

The single-channel x4 D351 card offers a bi-directional link speed of 10 Gbits/s. For greater bandwidth, the D350 and D352 cards use two bi-directional links, effectively doubling throughput to 20 Gbits/s. The low 1.4-microsecond application-to-application latency reduces the overhead of inter-node control messages, allowing scalability for multi-node applications.

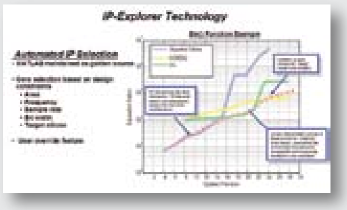
The cards' SCI links are hot-swappable connections. With the use of 2D/3D torus configurations or switches, SCI technology can be used to increase failover performance and fault tolerance. The cards support both direct memory access (DMA) and programmed remote memory access (RMA). Open-source software modules include SISCI API, MPICH and MPICH-2. In addition, Dolphin SuperSockets software for Linux and Windows allows the cards to be used without the need for application modification or recompiling. Pricing for single units begins at $1,005 for the D352.

Dolphin Interconnect Solutions, Sherman Oaks, CA. (818) 597-2114. [www.dolphinics.com].

DSP Synthesis Tool Automates IP Selection

Military designers implementing DSP algorithms in FPGAs and ASICs need extensive knowledge about how specific IP blocks will function in a given application. AccelChip's new IP-Explorer technology automates this process and has been combined with version 2005.4 of the company's DSP Synthesis software.

The combination accommodates macro-architectures or functional variants of mathematical building blocks such as sine, log and divide functions. Equipped with IP-Explorer, DSP Synthesis 2005.4 automatically selects and inserts the optimal AccelWare DSP IP implementation for each function in the design, based on a variety of system requirements such as frequency, throughput, bit-width, area and sample rate.



IP-Explorer utilizes heuristic modeling based on over 6,000 AccelChip and customer designs. AccelChip's automated IP development system runs all possible combinations of AccelWare DSP IP against these designs, using the latest versions of the most popular design tools to determine silicon results. The resulting database is used by IP-Explorer to select the optimal macro-architecture as the design's starting point. During product development the design is automatically updated to new architectures if required by changed system requirements. Pricing for Version 2005.4 of AccelChip DSP Synthesis with IP-Explorer starts at $15,000.

AccelChip, Milpitas, CA. (408) 943-0700. [www.accelchip.com].

16-Port USB-to-Serial Servers Connect Multiple Peripherals

Just a few years ago, the DoD gave USB its stamp of approval for use in military applications. Since then, the use of this interface has grown in defense designs. In systems where the host computer communicates simultaneously over multiple ports with varied peripheral types, it can quickly accumulate overhead. That overhead can be reduced considerably by a state-machine architecture, such as the one employed in the SeaLINK+16/232 and SeaLINK+16/485 16-Port USB-to-serial servers from Sealevel Systems.

Offering 16 independent serial ports, SeaLINK+16 devices can be used to connect multiple peripherals, such as barcode scanners, serial displays and data acquisition modules, to any USB port. The serial ports on each SeaLINK+16 appear as standard COM ports to the host system, enabling compatibility with legacy software. Data rates of up to 921.6 Kbits/s are supported, and the SeaLINK+16/485 offers RS-232/485 selectivity through cabling. Two USB 1.1 downstream connections are provided for daisychaining SeaLINK devices or interfacing standard USB peripherals.

The SeaLINK+16/232 and SeaLINK+16/485 ship with Sealevel Systems' SeaCOM suite of drivers for Windows 95/98/ME/NT/2000/XP. Also included is the WinSSD application for testing and diagnostics. Both models are housed in rugged 1U rackmount metal enclosures. Standard operating temperature range is 0° to 70°C, and extended temperature range (-40° to +85°C) models are available. Prices start at $729 for the SeaLINK+16/232.

Sealevel Systems, Liberty, SC. (864) 843-4343. [www.sealevel.com].

Flash Disk Delivers 80 Mbytes/s Sustained Transfer Rates

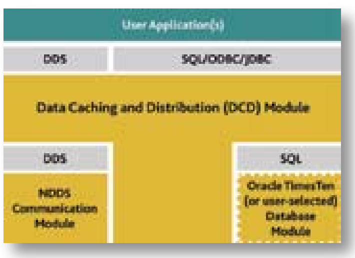
The netcentric battlefield is driving the need for very fast aggregation of large amounts of data for critical, real-time analysis. More and more defense application designers are looking at 3.5-inch form-factor solid-state storage during their design phase to get high capacities and high sustained data transfer speeds. With those applications in mind, Adtron has introduced the latest flash disk in its Flashpak family, the A35FB 3.5-in. Serial ATA (SATA) disk, with sustained data transfer rates of up to 80 Mbytes/s.

The company's ArrayPro technology gives the A35FB and other flash disks in the Flashpak family among the industry's highest sustained performance rates for a given capacity. Up to 128 Gbytes fit in a standard 3.5-in. form-factor. "Clear" and "sanitize" functions ensure rapid and secure data elimination from the media when required. Optional destroy, write protection and password protection features are also available. The A35FB flash disk supports either commercial (0° to 70°C) or industrial (-40° to +85°C) temperature ranges. Quantity pricing for an 8 Gbyte disk is $1,900.

Adtron, Phoenix, AZ. (602) 735-0300. [www.adtron.com].

High-Speed, Scaleable Framework Targets Distributed Data Management

Mission-critical, real-time distributed defense networking applications often depend on a data-centric publish-subscribe (DCPS) database system. These operate across an extendable network without the access bottlenecks associated with a central server-based model. The SkyBoard software framework for managing distributed data systems from Real-Time Innovations (RTI) combines Oracle/TimesTen's In-Memory Database, distributed database synchronization technology and RTI's Network Data Distribution Service (NDDS) communication middleware.



The Oracle/TimesTen In-Memory Database lets individual computer nodes keep complete copies of a database's data store units in local memory, reducing the need to move data to and from a disk during operations and resulting in fast data access of 35,000 transactions per second. RTI's technology synchronizes database copies on multiple nodes, enabling fast access throughout a distributed system regardless of the number of nodes. RTI's NDDS 4.0 connects the various elements and uses a DCPS model that simplifies complex, high-performance data distribution while controlling the quality-of-service parameters needed for real-time applications. The infrastructure includes an industry-standard SQL interface via ODBC libraries, simplifying application development and combining data from disparate systems for real-time or post processing and analysis.

SkyBoard includes all software elements (DDS APIs as well as the SQL/ODBC APIs), three developer toolkits for SkyBoard and a four-day product training program. Prices start at $75,930 for RTI's NDDS solution with SkyBoard for Solaris, Linux and Windows (beta version).

Real-Time Innovations, Santa Clara, CA. (408) 200-4700. [www.rti.com].

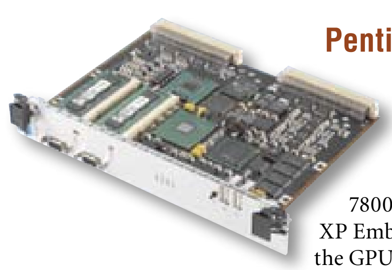
Generic, Off-the-Shelf DC-to-AC Evaluation Inverters

Defense applications continue to ramp up the use of complex graphical human-machine interfaces, driving the need for more LCDs. Military systems designers may need to quickly evaluate a DC-to-AC inverter that powers the CCF lamps backlighting LCDs. To fill that need, Endicott Research Group (ERG) has introduced the D Series Inverter, a family of generic, off-the-shelf inverters.

D Series inverters can be substituted for any of the company's specific standard inverters for most LCD modules and can be shipped from stock. They are the same size as the regular part and fill 90% of pre-production design requirements. Once production begins, the standard parts can be substituted and shipped under normal lead times.

D Series inverters such as the 2-lamp Model DLDS60J, based on ERG's LDS Series inverter, feature a low profile of less than 9 mm with display-compatible connectors, and are designed to generate 6 mA RMS into a 350V to 550V load from a nominal 12 VDC source. Operating temperatures are 0° to 70°C and onboard PWM dimming is included. Pricing in production quantities for the DLDS60J is $12.70.

Endicott Research Group, Endicott, NY. (800) 215-5866. [www.ergpower.com].



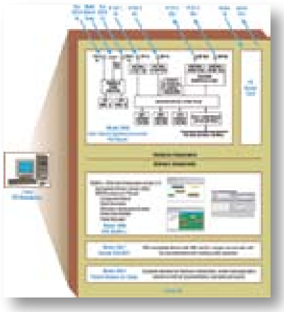
Pentium M-Based VME Graphics Card Delivers High Performance

Graphics-intensive aerospace and defense applications such as 3D terrain generation, embedded training and simulation consume the same huge amounts of data bandwidth needed for video games. The Screaming Eagle SE1 Pentium M-based graphics card from Radstone Embedded Computing brings the high-performance power of desktop gaming to aerospace and defense graphics systems.

Based on the Intel "Sonoma" architecture for high-performance drawing, the SE1 contains an nVidia GeForce 7800 GT graphics processing unit (GPU) driven by the 2.0 GHz "Dothan" Pentium M processor running Windows XP Embedded and the 915GM Northbridge chipset. The 16-lane PCI Express interface between the Northbridge and the GPU allows rendering of more vertices and textures.

The board features 2 Mbytes of on-chip Level 2 cache and a front-side bus speed of 533 MHz. The dual-slot 6U VME card includes 2x VME and 2eSST protocols, peak transfer rate of 320 Mbytes/s and backward compatibility with VME64X. Pricing for a single unit is $9,280.

Radstone Embedded Computing, Towcester, UK. +44 (0) 1327 359444. [www.radstone.com].



SDR Development Platform Is SCA-Compliant

Creating a reconfigurable radio that can be adapted to multiple radio standards without replacing hardware is the goal of the Joint Tactical Radio System (JTRS).

The SCA 2510 software defined radio platform from Pentek is geared toward developing interoperable applications and complies with the mandatory Software Communication Architecture (SCA) for U.S. military radios.

The SCA 2510's hardware platform is a Pentek 7640 dual-channel software radio transceiver PCI board installed in a PC workstation. Two 14-bit, 105 MHz A/D converters digitize HF or IF input signals and two 16-bit, 500 MHz D/A converters generate output signals. A Virtex-II Pro VP50 FPGA serves as a control and status engine with data and programming interfaces to onboard resources. Built-in buffering is achieved with 512 Mbytes of DDR SDRAM. The 64-bit/66 MHz PCI interface includes a nine-channel DMA controller.

The SCA 2510's software development environment supports Linux and is based on the SCARI++ SCA Core Framework, Component Development Library and Software Defined Radio Development Toolset, which is integrated with Pentek's SCA-compatible BSP. The GateFlow FPGA Design Kit extends the Virtex-II Pro's base functionality. The computer ships with Linux, development tools and the SCARI++ SCA core framework. Price starts at $85,000 for all hardware and software tools.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].

Serial ATA HDD Module Offers Higher Performance, Easy Configuration

Serial ATA's higher data transfer rates bring faster speeds to hard disk drives used in military embedded systems, while its use of high-speed serial cables make them easier to configure. Taking advantage of this fact is the PMC-0247 SATA hard disk drive module from GE Fanuc Embedded Systems.

The PMC-0247 is designed for use with GE Fanuc's SBCs or PMC expansion cards. With its support for universal signaling, the module can be installed in any available 3.3V or 5.0V PMC site. It uses a 2.5-in hard disk drive and has a maximum capacity of up to 80 Gbytes. The module supports a 32/64-bit, 133 MHz maximum PCI-X interface and a programmable external Flash for BIOS expansion.

Options include Serial ATA I or Serial ATA II-type drives, 40 Gbyte or 80 Gbyte capacities and standard or continuous operating modes. The module is compliant with VITA 39 and supports Windows 2000, Windows XP and Linux Enterprise 4.0. Prices start at $535.

GE Fanuc Embedded Systems, Huntsville, AL. (256) 880-0444. [www.gefanuc.com].

CompactPCI Express Backplanes Target Video Graphics Apps

A new generation of video graphics applications has come to military embedded computing, such as mobile defense subsystems in transportation systems. They all require higher performance, especially in backplanes, and that can be supplied by CompactPCI Express. The four-slot CompactPCI Express EXP0 backplane from Elma Bustronics has a 10-layer stripline design and contains a system slot, one Type 1 slot and two Type 2 slots.

Based on the new PICMG specification, the EXP0 backplane is backward compatible to CompactPCI and also supports next-generation PCI Express architecture in the familiar 6U-160 Eurocard form-factor. Cards are connected via a serial point-to-point bus with a read-only bandwidth of up to 2.5 Gbits/s (16x) or 2.5 Gbits/s full duplex (8x). Support for several different card form-factors are provided, with connectivity in 1x, 2x, 4x and 8x increments. Each link is 2.5 Gbits/s full duplex. Support of legacy 32- or 64-bit CompactPCI boards is accomplished by a PCIe-to-PCI bridge. Because the CompactPCI Express architecture supports the P3, P4 and P5 connectors in all 6U slot types, it can continue to support all existing CompactPCI secondary architectures, such as PICMG 2.5, 2.20, 2.16, 2.17 and 2.18, either as functions on native cPCI Express cards or as legacy cards in the original cPCI form.

Pricing for the 4-slot EXP0 backplane is under $400, depending on volume and configuration.

Elma Bustronic, Fremont, CA. (510) 490-7388. [www.elmabustronic.com].

RF Digital Tuning Modules Target COMINT, ELINT Apps

In communications intelligence (COMINT) and electronics intelligence (ELINT), quickly identifying signals of interest and locating a specific signal's origin are critical. This can be especially difficult when operatives use brief transmissions or rapid, unpredictable changes in frequency. A new family of RF digital tuning modules from Mercury Computer Systems enables rapid signal identification and location, fast tuning speed for tracking highly agile signals and a wide detection range.

The Echotek Series RF modules have highly accurate frequency measurement for precisely sorting different signals. Exceptional spurious free dynamic range (SFDR) delivers a much wider signal detection range and permits less ambiguous signal discrimination and sorting. The modules also feature low phase noise for better performance in direction finding and beam forming, and a 10-microsecond tuning speed for tracking highly agile signals.

The modules are available in 6U VME (3000TE and 5000TE) and 6U CompactPCI (3000CTE and 3000CSE) form-factors. The 6U VME solution is compatible with VME64, VME64x and Mercury's new RapidIO-based VXS (VITA 41) multicomputer. Single unit quantity pricing for the Echotek Series RF base model of the 3000TE tuner solution starts at $30,000.

Mercury Computer Systems, Chelmsford, MA. (978) 256-1300. [www.mc.com].

Optical Interconnects Brave Harsh Environments

When the goal is to blend high data rates and harsh environmental conditions, optical interconnection technology is the way to go. The Pro Beam connector series from Tyco Electronics is a fiber optic interconnect designed specifically for such needs. The precise expansion and collimation of the optical transmission allows for easy connector alignment and has very low sensitivity to thermal changes and contamination. Resistance to vibration and low-loss performance makes the expanded beam interface well suited for many aerospace, avionics, field communication, defense and other situations where harsh operating conditions exist.

The Pro Beam series of connectors has been expanded and shrunk in size to allow for several arrangements. First, the connector can be used with ARINC 600 and 404 shells in conjunction with appropriate inserts and holder blocks. Also, MIL-C-38999 shell size 11 can accept the Pro Beam Mini inserts. Performance attributes of the Pro Beam series connectors include typical insertion loss of 0.5 to 1.0 dB at 1300 nm (optical, multimode) or 0.5 to 1.0 dB at 1310 nm (optical single mode). Under $270 for volumes of 100 pieces, this includes the shell kit, the insert kit (up to four fibers), ferrule kits and, if applicable, the cable seal.

Tyco Electronics, Harrisburg, PA. (800) 522-6725. [www.tycoelectronics.com].

Compact DC/DC Converter Offers 25W Output

Military environments place some unique pressures on power system designs. Today the trend is toward more complete system solutions to serve those needs. Along such lines, Rantec Power Systems has expanded its HDM-LLP line of 270 VDC input MIL-STD-704 compliant DC/DC converters, with the addition of a 25W output module. The feature-rich DC/DC converter is intended for applications requiring input to output isolation, low weight (no potting), ultra low radiated emissions (shielded), superior dynamic line and load performance, tactical military environmental conditions and operating temperatures of -55° to 95°C. Standard output voltages from 3.3 to 28 VDC are available. Tailored output voltages, overcurrent and overvoltage set points can also be configured.

The device's compact size and high performance make it an ideal element for a distributed power system. The HDM-LLP uses secondary side controls for precision overcurrent/over-voltage protection set points, superior dynamic line/load response and regulation. Using fixed frequency switching technology, HDM series converters incorporate power MOSFETs, planar magnetics and surface mount technology onto a metal clad PC board. The shielded module has excellent radiated emissions performance over a non-shielded module, translating to trouble-free system integration. Price is $196 each for 100 pieces.

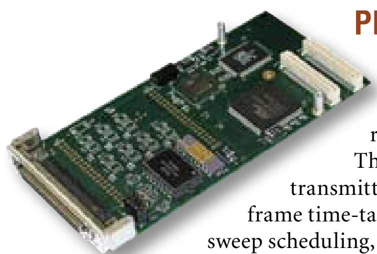
Rantec Power Systems, Los Osos, CA. (805) 596-6000. [www.rantec.com].

Tool Supports JTAG and Flash for Freescale and MIPS

The Freescale MPC5200 rev. B processor and the Freescale 83xx PowerQUICC II Pro family of processors both continue to gain interest among military system developers. Macraigor Systems now offers JTAG debug and Flash programming support for several new Freescale PowerPC and MIPS Technologies 64-bit processors. Full JTAG debug and Flash programming support has been added for those processors. In addition, Macraigor's Flash Programming application has been updated to support the Freescale MPC5500 and MAC71xx families of processors along with MIPS 5kc-based 64-bit processors from Phillips, Toshiba and Broadcom.

Macraigor has also added support for those processors to the free, pre-built GNU tools suite to include sample configurations for standard evaluation boards. These examples contain source, gdbinit and make files for each board. The included demo program allows developers to easily build, download and debug a small application via gdb. OCDemon Flash Programmer, Flash Access and Target Access are each $500 for the first license, and incremental licenses are $100 each. OCD Commander, an assembly-level software debugger, and OCD Remote, the GNU tools suite, are available at no charge from the Macraigor website.

Macraigor Systems, Brookline Village, MA. (617) 739-8693. [www.macraigor.com].

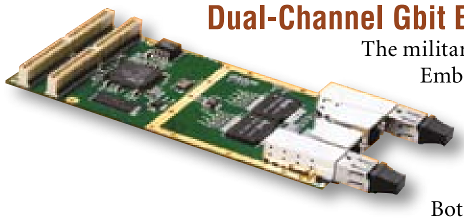


PMC Serves Up Dual Channel ARINC 708 Buses

The PMC mezzanine form-factor is perhaps the most popular tool for mixing and matching I/O functionality in military systems. Condor Engineering has migrated its ARINC 708 interface technology to the more versatile PMC module. Called the P-708, this ARINC 708 databus interface is designed for weather radar applications.

The P-708 simultaneously supports two ARINC 708 channels. Each P-708 channel operates as an independent transmitter or receiver with programmable frame size and buffer storage capacity. Specialized receive features such as frame time-tagging and error detection/notification of short/long frames, as well as specialized transmit features such as sweep scheduling, programmable frame gap duration, and short/long frame and start/stop sync error injection, are included. With a programmable number of bits per frame, the P-708 is useful for a wide range of 1 MHz Manchester-encoded applications. Condor provides integrated support for this module on PCI, CompactPCI, VME, VXI and native PMC platforms. An easy-to-use, high-level software API (Application Programming Interface), is included with support for Windows XP, 2000, Me, NT, 98, 95 and VxWorks (x86 and PPC). The API is also provided in C source code for ease of integration. Pricing for the dual channel ARINC 708 P-708 is from $2,800.

Condor Engineering, Santa Barbara, CA. (805) 965-8000. [www.condoreng.com].



Dual-Channel Gbit Ethernet Climbs Aboard PMC

The military's affection for Ethernet shows no sign of waning. Feeding that trend, Curtiss-Wright Controls Embedded Computing has introduced the PGE2, a new dual-port Gbit Ethernet PMC card. Powered by an Intel 82546EB Gbit Ethernet Controller, the PGE2 is fully compatible with legacy 10/100BASE-TX networks and simplifies the addition of Gbit Ethernet networking into existing VME, CompactPCI or PCI embedded systems.

This new Gbit Ethernet PMC card is available in both air-cooled and conduction-cooled versions. Both cards boast a humidity spec of 10-95% RH non-condensing. The air-cooled PGE2 comes with a standard operating temperature of 0° to +50°C. It supports either single or dual 10/100/1000BaseTX using standard RJ-45 connectors or optical 1000BaseLX interfaces with LC-type fiber connectors. An extended-temperature air-cooled range version is also available and operates at -40° to +71° C, using forced air cooling. The conduction-cooled version of the card is specified for operation over a range of -40° to +85°C and provides support for single or dual 10/100/1000BaseTX interfaces for host board backplane connections. Pricing for the PGE2 starts at $1,364.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

Win CE Dev Kit Targets XScale and Geode Designs

Windows CE is popular for any embedded application requiring a user interface, and military designs are no exception. Arcom, a Gold-level Windows Embedded Partner, has released updated Development Kits for two embedded single board computers—the ultra-low power 400 MHz PXA255 XScale-based VIPER and the AMD Geode-based SBC-GX1. These development kits save months of engineering time and BSP integration effort by offering Windows CE 5.0 on a ready-to-run platform. The kits include the VIPER or SBC-GX1 pre-installed with Windows CE 5.0 on the resident flash drive as well as the Microsoft eMbedded Visual tools to allow developers to start building an application right away.

The VIPER Development Kit includes the VIPER PC/104 board fitted with 64 Mbytes DRAM and 32 Mbytes of flash memory and an industrial compact enclosure (ICE) with a Q-VGA color touchscreen display. The Development Kit is also shipped with a free CompactFlash Wi-Fi card allowing complete wireless operation. The 300 MHz SBC-GX1 EBX board is fitted with 256 Mbytes DRAM and 16 Mbytes of onboard flash, along with a 6.5-in. VGA TFT touchscreen display. Both are priced at $1,597.

Arcom, Overland Park, KS. (888) 941-2224. [www.arcom.com].

USB Digital I/O Card Features PC/104 Mounting Scheme

It took a while for USB to find its way from the desktop to the embedded space, much less to the military embedded market. But now it's an accepted technology. Supporting that acceptance is ACCES I/O Products' latest embedded digital I/O board packaged in a small, rugged, industrial enclosure—the Model USB-IIRO-16. Featuring 16 Form C (SPDT) electromechanical relays and 16 optically isolated digital inputs, the unit is a very dense, portable, embedded solution.

The unit contains an internal, removable screw termination board with onboard removable screw terminals to simplify wiring connections.

The USB-IIRO-16, like the PC/104 and PCI versions from ACCES I/O, is excellent in applications where onboard relays are required and inputs must be isolated such as in test equipment, instrumentation, and process control. The board's size and mounting holes match the PC/104 form-factor (without the bus connections). This allows our rugged digital board to be added to any PCI-104 or PC/104 stack by connecting it to a simple USB port usually included onboard with embedded CPU form-factors such as EBX, EPIC and PC/104—especially important since many newer CPU chipsets do not support ISA and have plenty of USB ports. Available now, the USB-IIRO-16 is priced at $349.

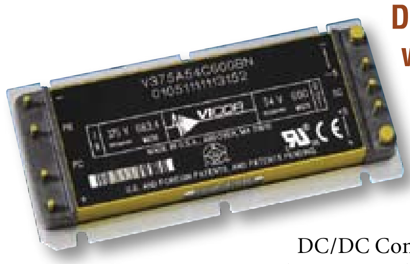
ACCES I/O Products, San Diego, CA. (858) 550-9559. [www.accesio.com].

Mountable Computer Sports Detachable Display

Embedded computers and LCD panels don't necessarily require upgrade or repair at the same times. Therefore, it's helpful to replace one without having to swap out the other. That's the thinking behind Arista LCD Panel Computers. Its latest addition to that product line is the ARP-1720AP Panel Computer featuring a NEMA 4 Panel Mount 20.1-inch LCD. The ARP-1720AP has a modular computer unit that is detachable and easily removed from the display. This provides the user easy maintenance and the ability to quickly upgrade the unit.

The ARP-1720AP series is designed for flexibility, versatility, easy servicing and quick upgradeability. With a detachable panel mount LCD monitor and modular computer unit, a variety of configurations are easily achieved. The ARP-1720AP allows users the flexibility of swapping the computer module or LCD display with the simple removal of four screws. The unit provides a variety of configurations ranging from a PIII CPU to a powerful P4 CPU. The ARP-1720AP can also be configured with a DC24V or 100~230 VAC input power supply. Multiple expansion slots and an optional RAID-1 are available for certain configuration. Pricing for the ARP-1720AP series starts at $4,000.

Arista, Fremont, CA. (510) 226-1800. [www.aristaipc.com].



DCDC Converter Brick Delivers 600W with 54V Outputs

Because they prefer to think in terms of separate modular blocks, military system designers were slow to warm to the idea of distributed power. Now it's a requirement in all systems, including high power density environments. Serving that need, Vicor has announced the release of a new 375 Vin, 54 Vout DC/DC Converter Module, the V375A54C600B, first of a planned expansion of its matrix of 375 Vin high power density DC/DC converters. All have an input range of 250 to 425 VDC and have power densities ranging from 80 to 120 W/cubic inch. This release extends the full brick "Maxi" output voltage range to 54 Vout. The output power is 600W.

The 375V family comprises three package sizes—full, half and quarter-brick (Maxi, Mini and Micro)—each offering output voltages of 2, 3.3, 5, 12, 15, 24, 28, 48 and now 54 VDC for the Maxi package. The family offers output powers from 50 to 600 watts. All of the modules incorporate the same advanced features as other Vicor 2nd Generation DC/DC converters, such as high-density packaging, high temperature rating, wide output voltage trim range and paralleling for higher power and redundancy. Pricing for the V375A54C600B is as low as $0.29 per watt in quantities of 1,000.

Vicor, Andover, MA. 800-735-6200. [www.vicorpower.com].

Signal Generator Supports Low Phase Noise Capability

To properly evaluate signals critical for military applications—like high-resolution radar and RF comms subsystem design—you need a signal generator capable of ultra-low phase noise performance and outstanding spectral purity. Along those lines, Agilent Technologies has introduced an ultra-low phase noise option for the PSG vector and analog signal generators, providing the lowest phase noise capability for signal generation in the industry. Agilent also announced a new frequency range option for its PSG analog signal generator. Providing coverage over the 250 kHz to 31.8 GHz frequency range, this option now offers RF engineers a cost-effective choice for applications up to 31.8 GHz.

Agilent's ultra-low phase noise capability, Option UNX, offers a phase noise performance of -111 dBc/Hz at a 100 Hz offset and -133 dBc/Hz at a 10 kHz offset on a 1 GHz carrier frequency. Agilent's new 31.8 GHz frequency range option for the PSG analog signal generator, Option 532, provides design engineers working in satellite communications and other K-band applications a flexible and affordable alternative to higher-frequency signal generators. Available now, pricing for the ultra-low phase noise option for the Agilent PSG analog signal generators ranges from $12,700 to $32,500.

Agilent Technologies, Palo Alto, CA. (408) 654-8675. [www.agilent.com].

Enclosed Celeron M SBC Boasts Fanless Operation

As a general rule, fan-cooled computing systems are frowned upon by all but the most benign military applications. Serving the need for low-power, fanless operation, WIN Enterprises offers an enclosed computer designed for the embedded OEMs designing applications for harsh environments. The PL-06058 is powered by an 34W Intel Celeron M ULV or Pentium M processor with low power requirements. The fanless unit provides silent operation where ambient noise is unwanted. Internal heat pipes conduct heat to the aggressive heat-sink design of the rugged aluminum enclosure.

The PL-06058 is an enclosed version of WIN's popular IP-06058 single board computer (SBC). The PL-06058 is suited for scientific, military and aerospace applications. The compact unit supports a CompactFlash socket, Mini-PCI slot and up to 1 Gbyte of DDR RAM. Also featured are: one 10/100 Ethernet port, four serial ports, one parallel port, an IDE interface, three USB 2.0 ports and a FDD interface packaged into an industrial grade enclosure of 12.3 (width) x 5.5 (depth) x 2.6 (height) inches. Pricing for the PL-06058 ranges from $533 to $552.

WIN Enterprises, N. Andover, MA. (978) 688-2000. [www.win-ent.com].

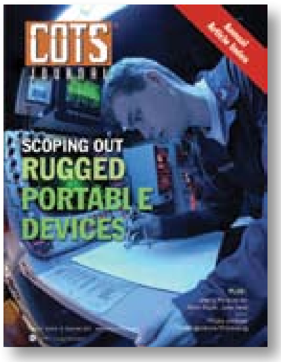
Rugged Vehicle Computer Weighs a Mere Six Pounds

Cramming as much compute density as possible into a small space is the name of the game for systems such as UAVs and ground combat vehicles as well as portable computing units for troop field use. SBS Technologies continues to push that integration curve by introducing a versatile Rugged Operational Computer (ROC). The ruggedized ROC vehicle computer is a powerful and compact PMC computing system. Weighing less than six pounds and measuring less than 100 cubic inches, the ROC fits well into the tight spaces usually found in military vehicle applications. The ROC can be configured with an Intel or PowerPC processor PMC.

The ROC chassis has a modular stacked PMC architecture, an integrated 100W power supply and EMI filter, and a solid-state fast Compact Flash disk with up to 128 Gbytes of memory mounted on a PMC carrier module. Available now, pricing for one ROC System Enclosure, which includes one system chassis, one power supply and one single board computer, starts at $19,750. A two-ROC System Enclosure, which includes two system chassis, one power supply, one single board computer, one 8-channel high-speed serial PMC and one dual redundant MIL-STD 1553 PMC, starts at $44,500.

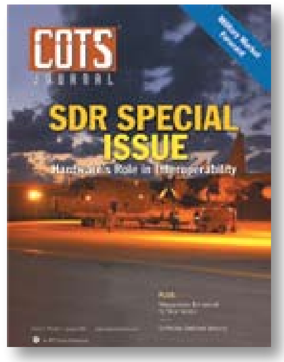
SBS Technologies, Albuquerque, NM. (505) 875-0600. [www.sbs.com].

December 2004



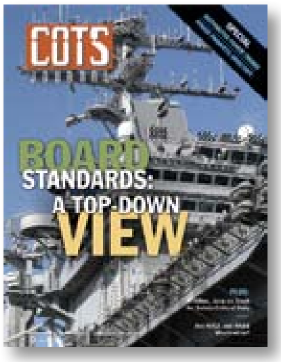
Scoping Out Rugged Portable Devices

January 2005



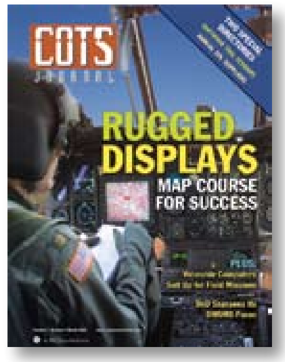
SDR Special Issue: Hardware's Role in Interoperability

February 2005



Board Standards: A Top-Down View

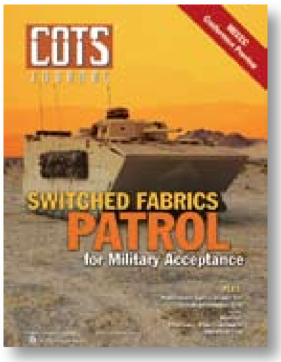
March 2005



Rugged Displays Map Course for Success

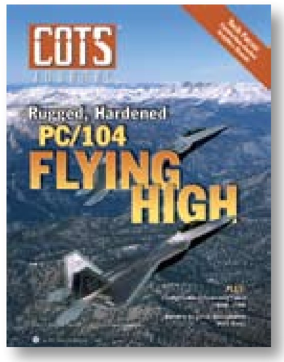
Annual Article Index

April 2005



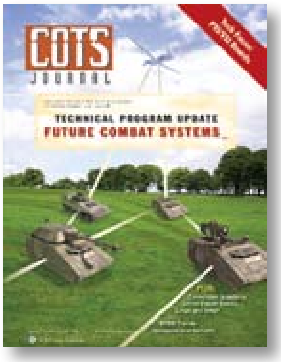
Switched Fabrics Patrol for Military Acceptance

May 2005



Rugged, Hardened PC/104 Flying High

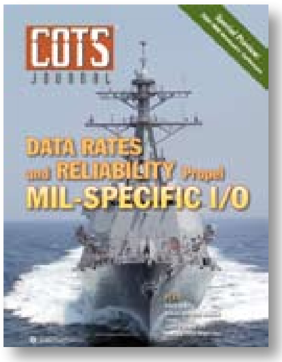
June 2005



Technical Program Update: Future Combat Systems

Annual Article Index

July 2005

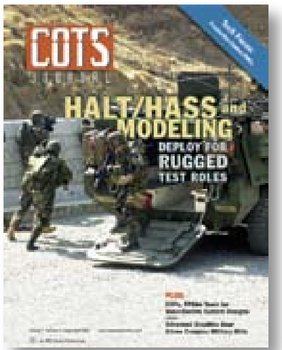


Data Rates and Reliability Propel MIL-Specific I/O

August 2005

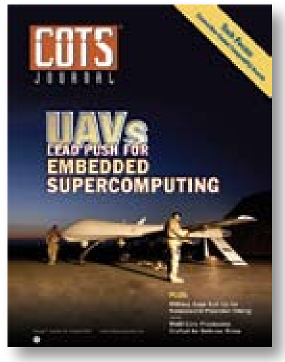
Gigabit Switching Fuels Ethernet Acceptance

September 2005



HALT/HASS and Modeling Deploy for Rugged Test Roles

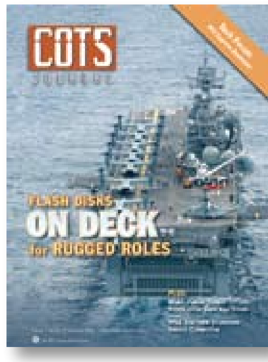
October 2005



UAVs Lead Push for Embedded Supercomputing

Annual Article Index

November 2005



Flash Disks on Deck for Rugged Roles

Advertisers Index

Get Connected with technology and companies providing solutions now

Get Connected is a new resource for further exploration into products, technologies and companies. Whether your goal is to research the latest datasheet from a company, speak directly with an Application Engineer, or jump to a company's technical page, the goal of Get Connected is to put you in touch with the right resource. Whichever level of service you require for whatever type of technology, Get Connected will help you connect with the companies and products you are searching for.

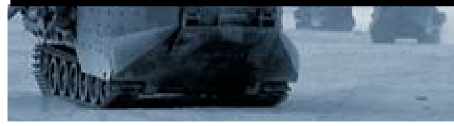
www.cotsjournalonline.com/getconnected

COTS Journal (ISSN#1526-4653) is published monthly at 905 Calle Amanecer, Suite 250, San Clemente, CA 92673. Periodicals Class postage paid at San Clemente and additional mailing offices. POSTMASTER: Send address changes to COTS Journal, 905 Calle Amanecer, Ste. 250, San Clemente, CA 92673.

Coming Next Month

Our editorial team started brainstorming article topics for 2006 way back in the summer. We're predicting 2006 will be the most exciting year ever for *COTS Journal*, so we've been chomping at the bit for the New Year to arrive. Now it's upon us, and here's what we've got cooking for you to feast on in our January issue:

- *Five Technologies Challenging the Military.* The U.S. Military faces some major technology challenges as it strives to meet its lofty goals—goals like complete sensor-to-shooter networked-centric operation and an ever-increasing reliance on autonomous unmanned land and air assets. For this special section, we'll analyze five areas that pose the most significant technology challenges facing today's military system designer. These include multicore processors, switched fabrics, FPGAs in configurable computing, managing and controlling UAVs, and Java.
- *Military Market Update and Forecast.* The military market hasn't quite met expectations, but still remains active. In this section we look at the market for a broad cross-section of military and aerospace embedded-computer applications. The update will also look at where some of the major programs are going and speculate on the probability of their success.
- *Rugged Displays.* By leveraging advanced commercial graphics silicon targeted for PCs and game boxes, military graphics subsystem integrators are able to provide a wealth of display controller features mostly in PMC form-factors or smaller. Articles in this section focus on trends in rugged displays and the subsystems that drive them.
- *PC/104 in the Military.* With its blend of compact size and inherent ruggedness, PC/104 continues to gain fans in the military realm. This Tech Focus section updates readers on PC/104 SBC boards and provides a product album of representative PC/104 SBC products. A special expanded product directory of PC/104 boards will be provided on our Web site.



COTS

Editorial

Jeff Child, Editor-in-Chief

IPv6: The Defense Industry Leads the Way

An often-quoted article penned a few years back by Marc Prensky, author of the book *Digital Game-Based Learning*, coined the terms Digital Natives and Digital Immigrants to describe the generation gap straddling the digital era. The basic idea is today's generation of kids were born and raised in a digital world of computers, the Internet, cell phones, CDs, DVDs, mp3 players and so on. In contrast, the people of the older generation are immigrants to this era, and are less comfortable adapting in it. If you're someone who prints out their emails before reading them—or have your secretary print them out—you're definitely a Digital Immigrant.

The same digital generation gap trend is affecting the U.S. Military. What's happening there—using Army ranks as an example—is that 1st and 2nd Lieutenants tend be the Digital Natives and more comfortable with computers, networks and all things digital. Those officers, now roughly in their late 30s or early 40s, are now moving up into the Colonel and Lt. Colonel ranks and having more influence as a consequence. Their comfort level with net-centric technologies is critical fuel for the DoD's broad vision of its Network-centric future.

That future calls for a real-time sharing of voice, video and data between soldiers, aircraft, satellites, ships, robots and UAVs all over a global network. Within that scope is the idea of doing all communications—voice, data and video—over Internet Protocol—or Everything over IP (EOIP) as the term is called. Certainly there are other ways aside from IP to implement such comms capabilities, but the EOIP idea seems to be winning out over alternatives.

A critical part of that is the move from Internet Protocol version 4 (IPv4) to Internet Protocol version 6 (IPv6). The DoD announced its transition strategy to IPv6 in 2003, requiring that all future network gear purchases be IPv4- and IPv6-capable, with a goal of full IPv6-compliance by 2008. The current Internet Protocol, IPv4, designed in the 1970s, was thought to have ample IP addresses for computers to connect to the Internet. With 32-bit addressing, IPv4 allows a maximum of roughly four billion addresses. That seemed like plenty in the 1970s, when bandwidth was limited and the Internet was virtually unknown to the general public.

Today, with the U.S. using about 75% of the available IPv4 address space, there's a real shortage of addresses for Asia and other regions. That combined with the extraordinary jump in the number of devices that can now be connected to the Internet means that IPv4's limited address space isn't enough to allow every device a unique IP address. Solutions like network address translation help ease the problem, but that adds complexity. IPv6 in contrast offers virtually an unlimited number of IP addresses—in fact the number is hard to image: nearly 600 quadrillion addresses for every square millimeter on earth.

By allowing each device to have its own unique global IP address, network address translation is no longer necessary; peer-to-peer communication will become much easier. Two devices will be able to establish direct communication without the need to translate between global and private addresses. Two-way applications such as IP telephony and video conferencing become much simpler to develop. Routing tables will become far less complex, which will enable higher performance for Internet traffic and more bandwidth for additional communication.

IPv6 comes with its own security protocol, IPsec. The security offered by IPsec comes into play at the IP layer of the TCP/IP stack. Because IPsec is applied at such a low level, there is inherent protection for all higher-level protocols, such as TCP, http, proprietary application protocols, and so on. The full payoff with IPv6 for the military is its ability to provide IP peer-to-peer connections for embedded systems. If the various electronic subsystems in an aircraft wing, for example, have their own IP address, diagnostic data about it's status could be accessed while the aircraft is in flight.

What's unique about the shift to IPv6 is that, unlike other technology areas, the Defense industry can't wait to follow the commercial and consumer markets. Partly, because the network address translation technologies are so mature and efficient, the enterprise market has been slow and lackluster in its shift to IPv6. Sure there's been lots of talk in the embedded market as to when household appliances, security alarms and automobiles will be connecting to the Internet. But that reality has been slow to evolve.

The DoD and the defense industry—as respectively—the world's most demanding customer and suppliers for complex, net-connected systems, have an opportunity to lead the way to an IPv6 world of everything connected. The good news is that they seem on track to do just that, and the military's Digital Natives—and forward thinking Digital Immigrants—are in the driver's seat. ▮